

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U37C

Clarkfield/Auburndale

DDR SYSTEM MEMORY A

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

DM signals are not present on Clarkfield
processor. All DM signal can be left as
NC on Clarkfield and connect directly to
GND on So-DIMM side for Clarkfield
design only

U37D

Clarkfield/Auburndale

DDR SYSTEM MEMORY - B

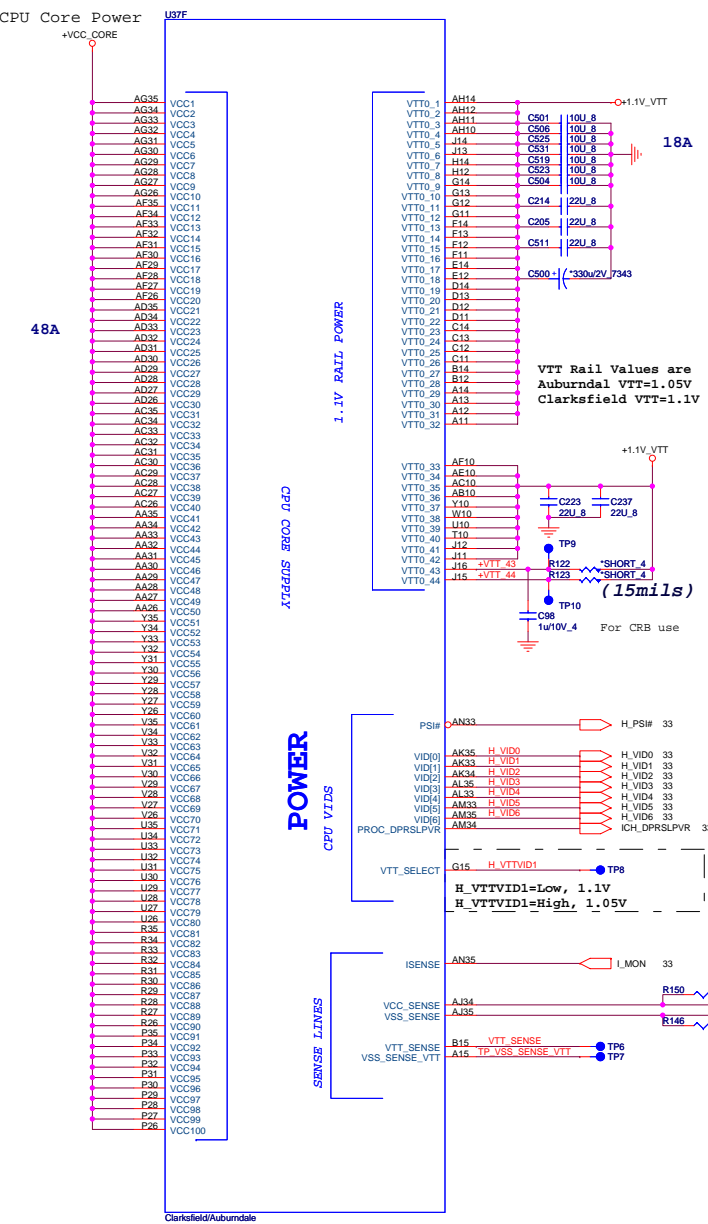
Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



Quanta Computer Inc.

PROJECT : ZY9

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

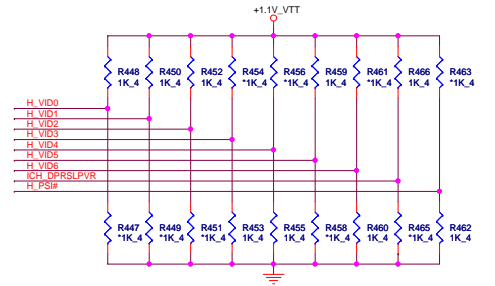


18A

VTT Rail Values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

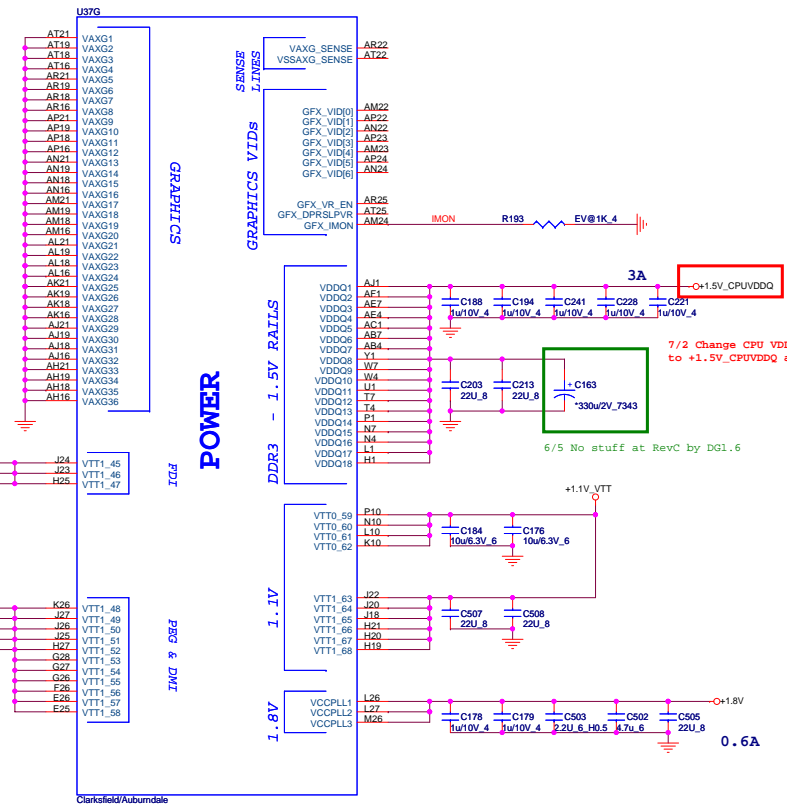
(15mils)

For CRB use



Note:
For Validating INVP VR R451 should be ST0VF
and R201 NO_ST0VF

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V



3A

7/2 Change CPU VDDQ from +1.5V_S3
to +1.5V_CPUVDDQ at c test.

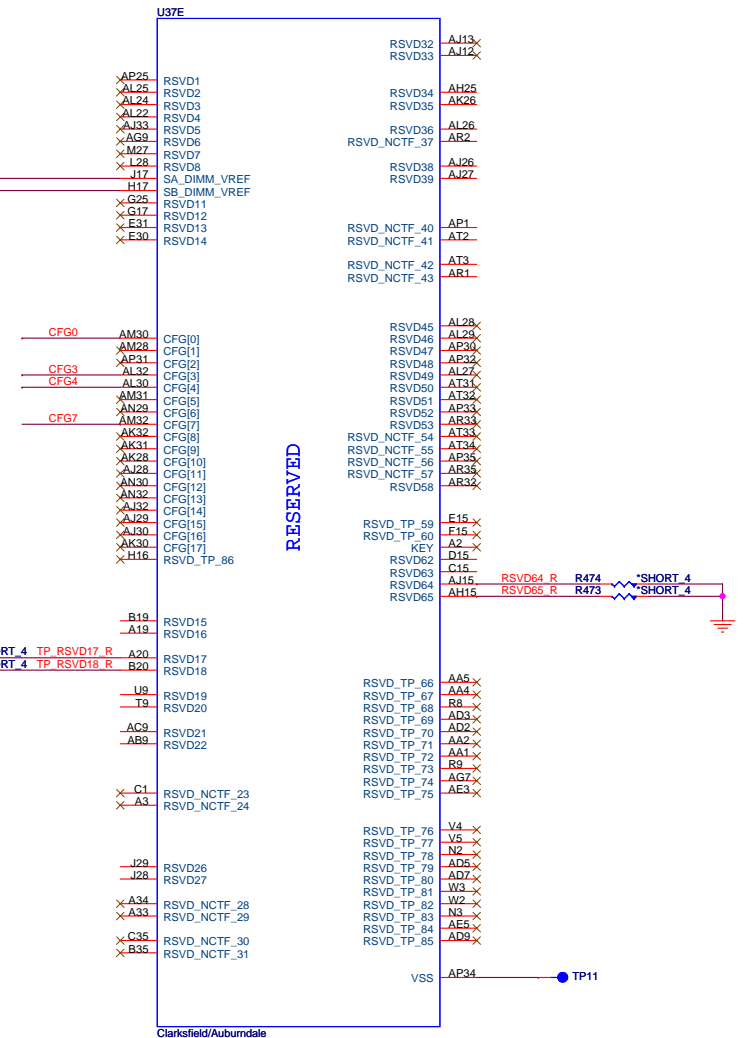
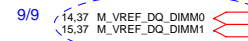
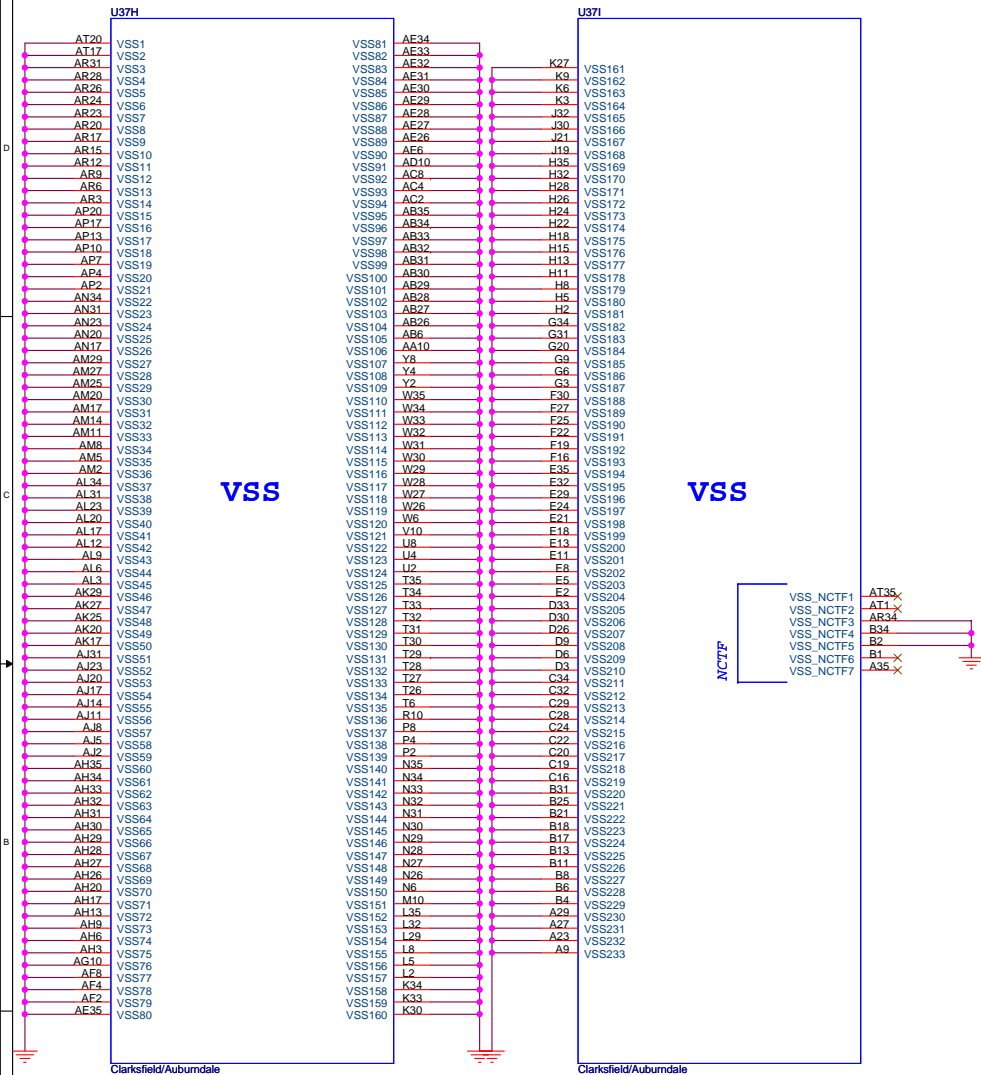
6/5 No stuff at RevC by DGI.6

0.6A

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

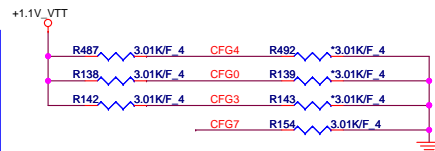
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

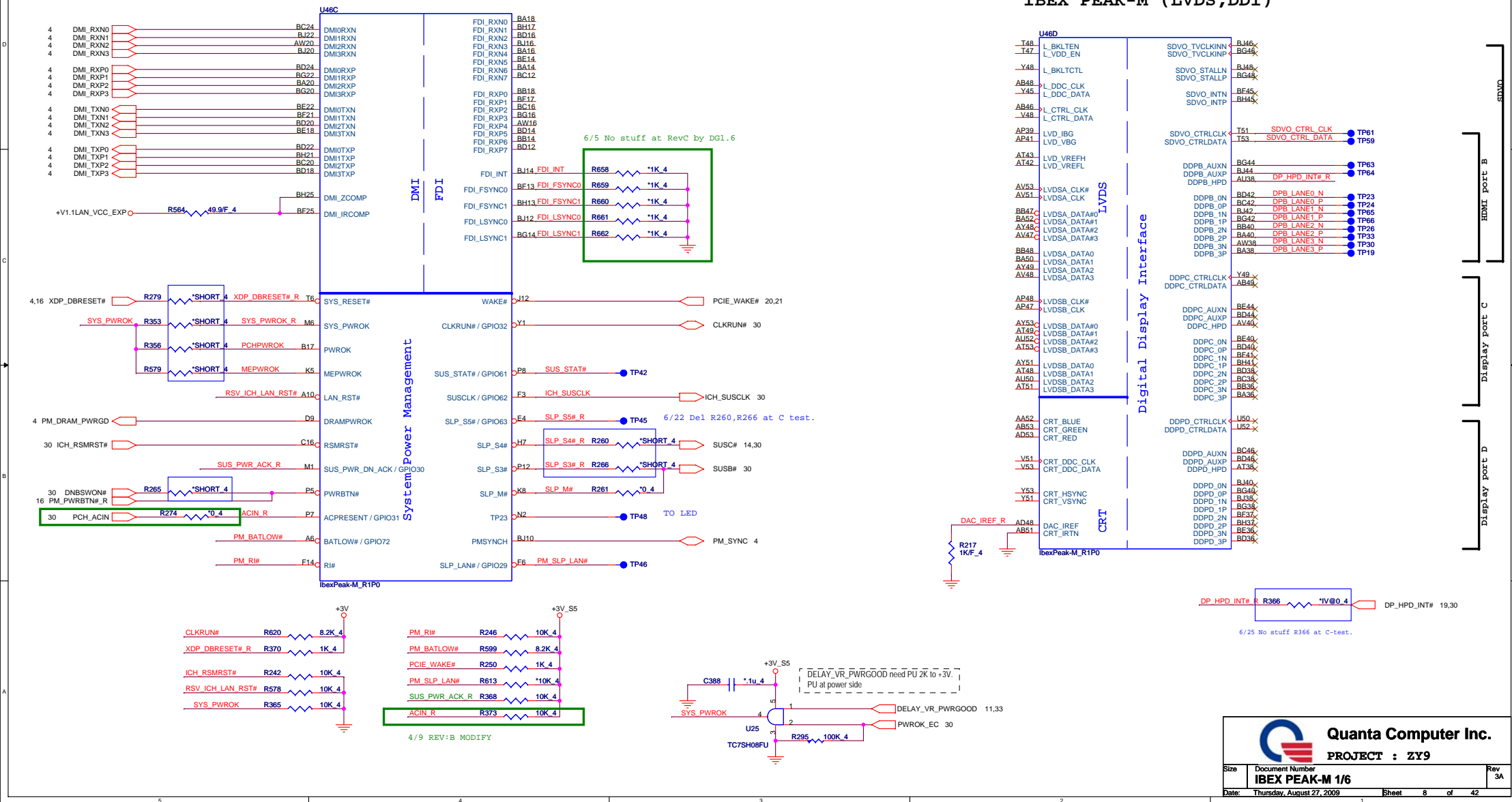
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The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



IBEX PEAK-M (LVDS,DDI)

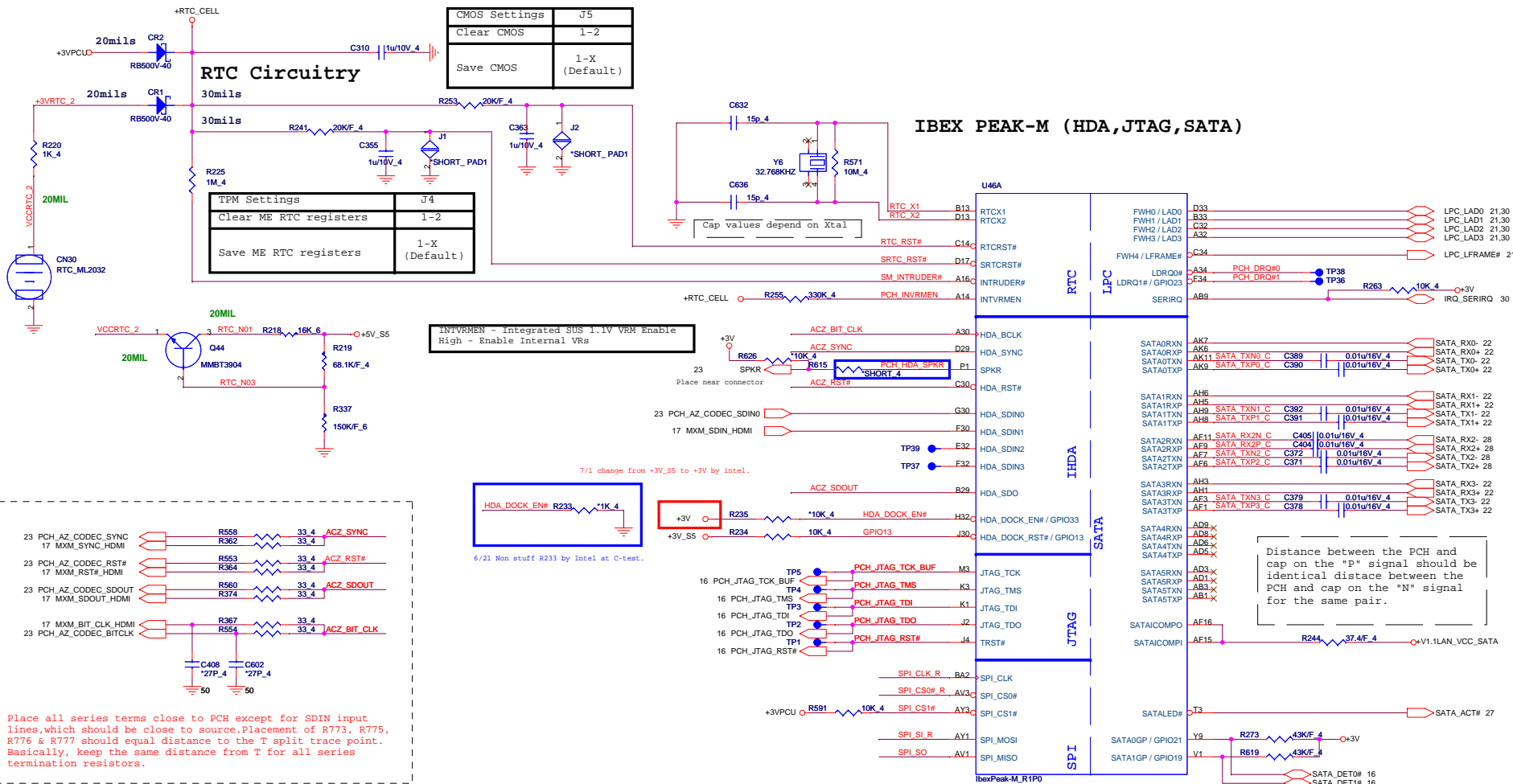


RTC Circuitry

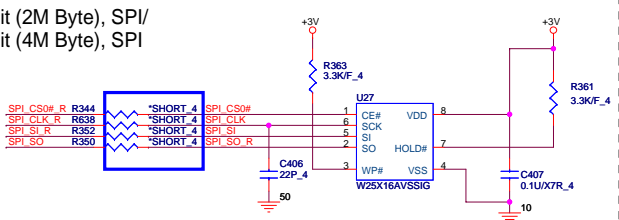
CMOS Settings	J5
Clear CMOS	1-2
Save CMOS	1-X (Default)

TPM Settings	J4
Clear ME RTC registers	1-2
Save ME RTC registers	1-X (Default)

IBEX PEAK-M (HDA,JTAG,SATA)



For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



iTPM ENABLE/DISABLE

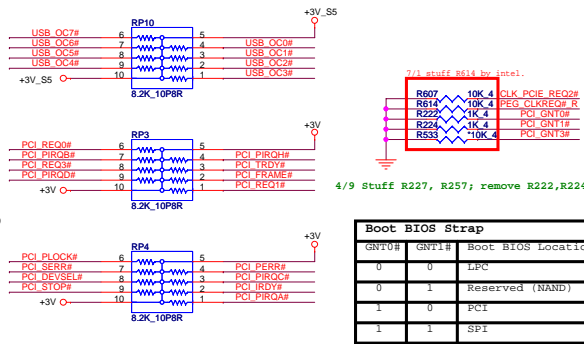
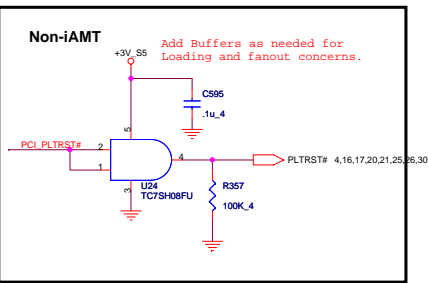
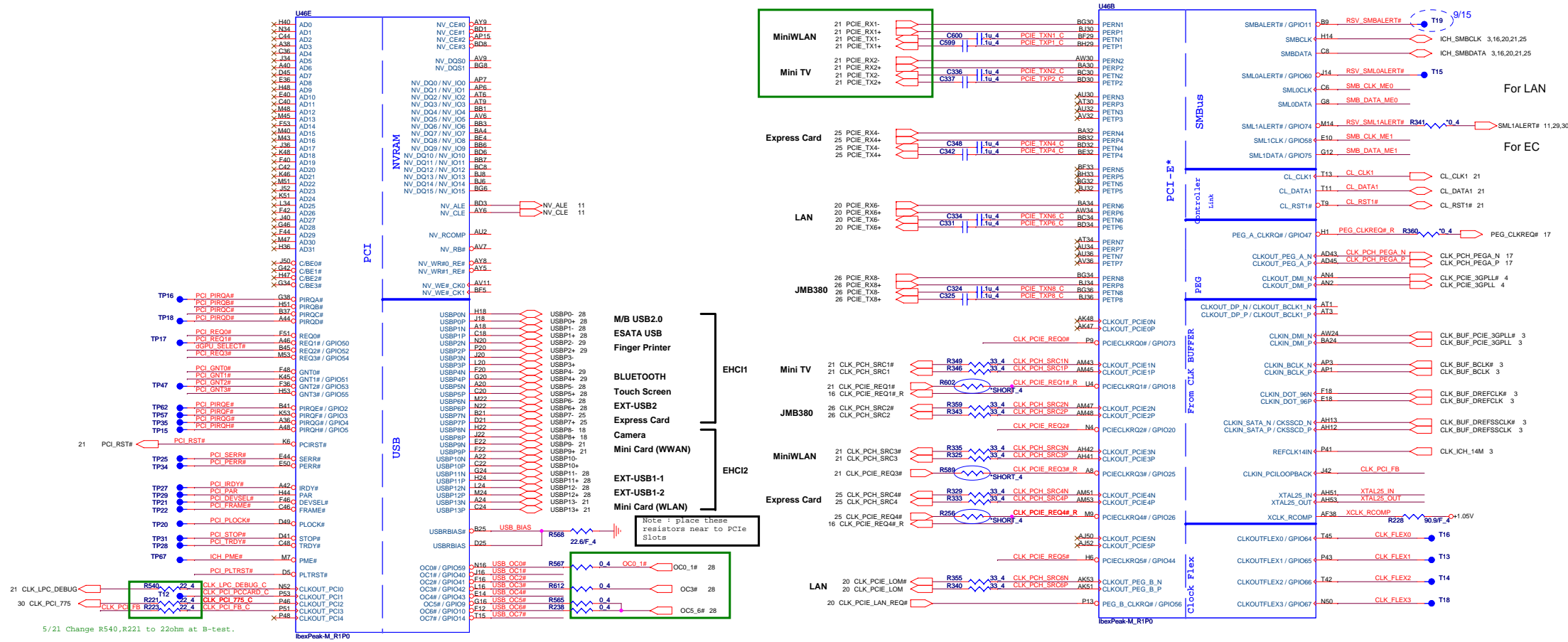
TPM Function	R591
Enable	Mount
Disable	NC (Default)

SATA_DET1# R369 "0_4" dGPU_EDIDSEL# 19

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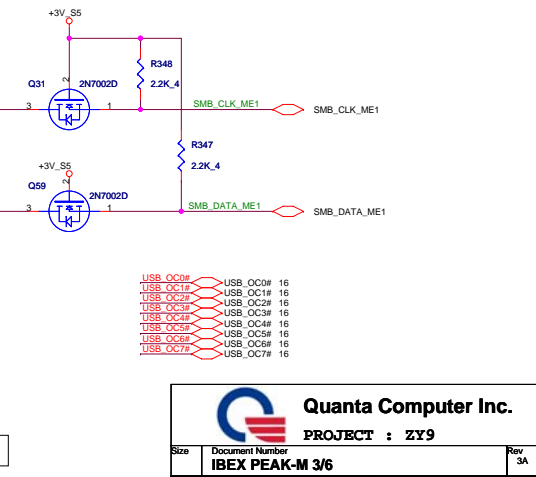
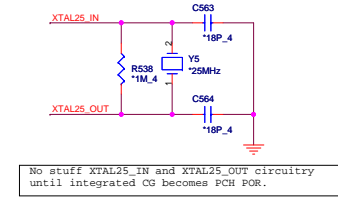
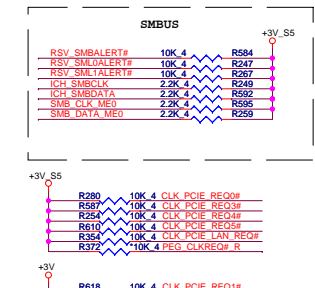
Size Document Number
IBEX PEAK-M 2/6

Date: Thursday, August 27, 2009 Sheet 9 of 42 Rev 3A

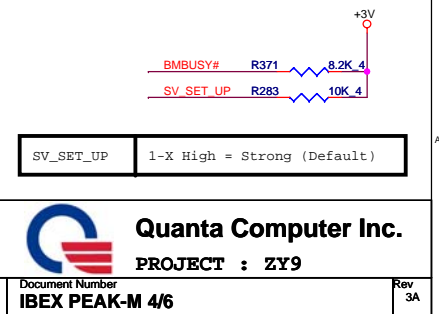
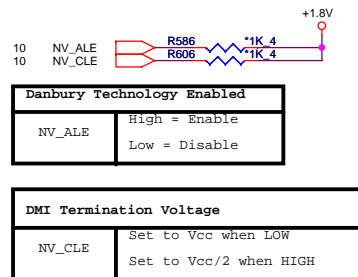
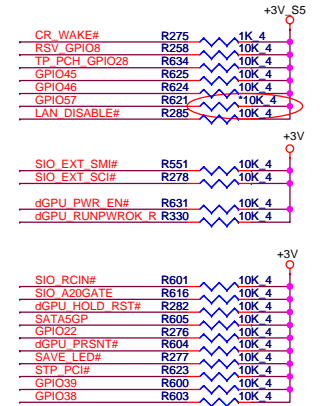


Boot BIOS Strap		
GN10#	GN11#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

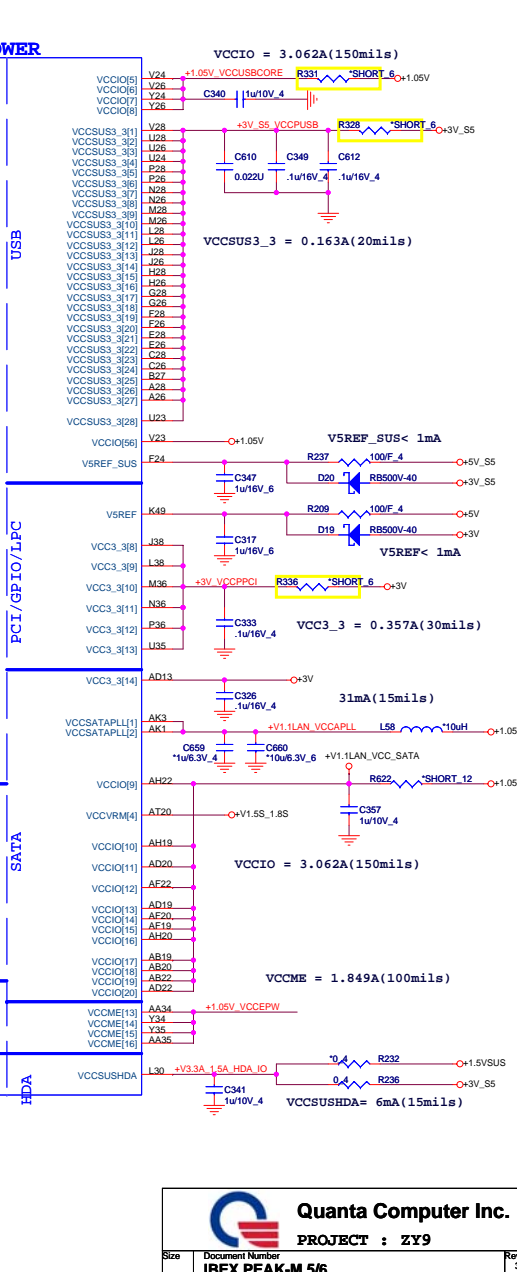
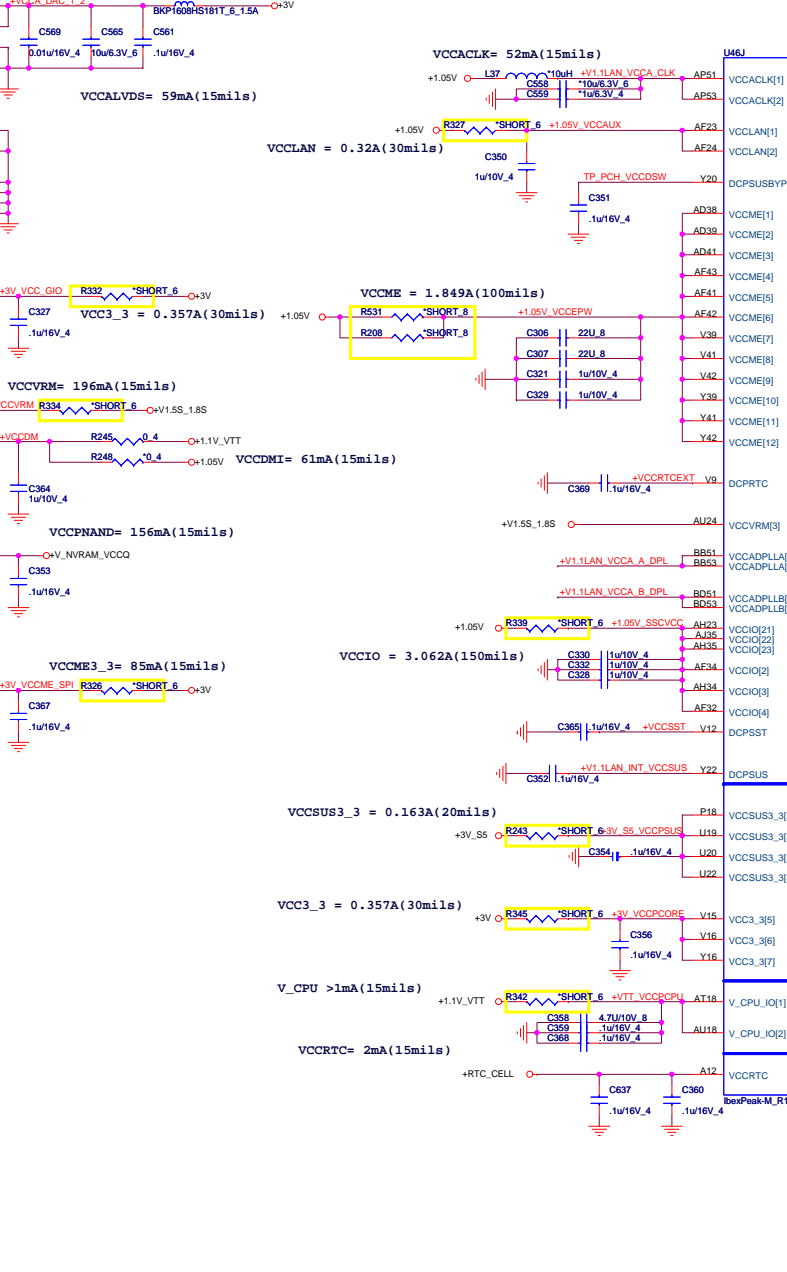
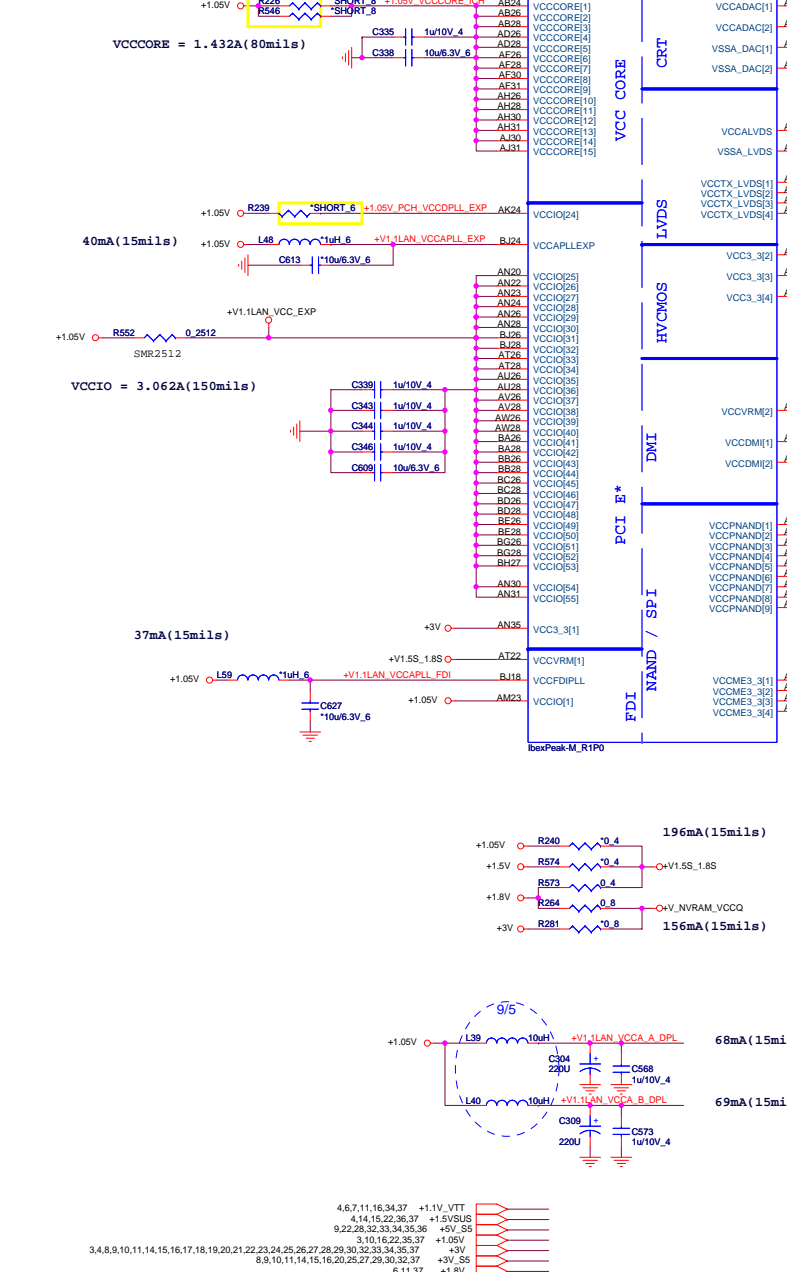
Alt6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	
LOW = Alt6 swap override/Top-Block Swap Override enabled	
High = Default	



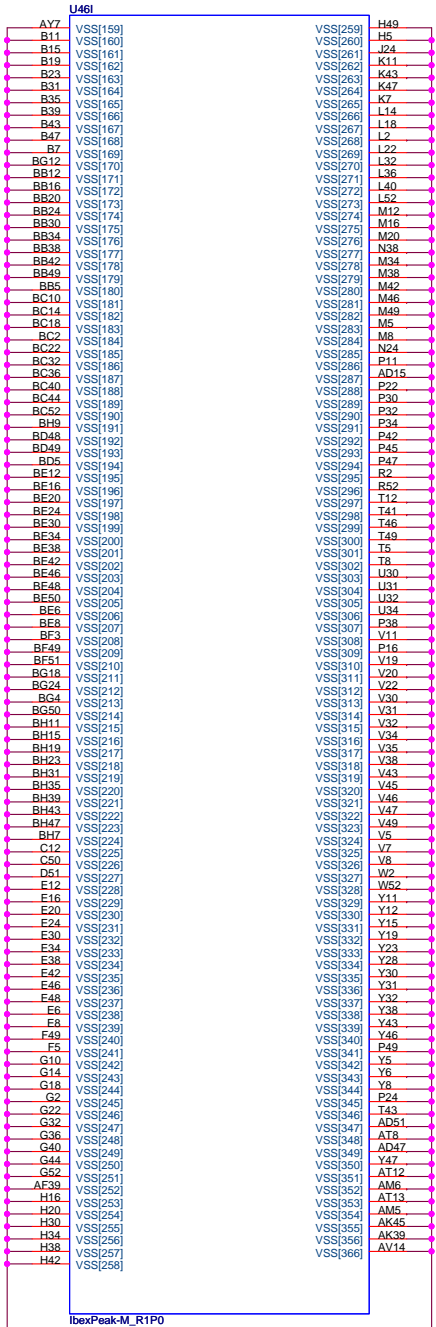
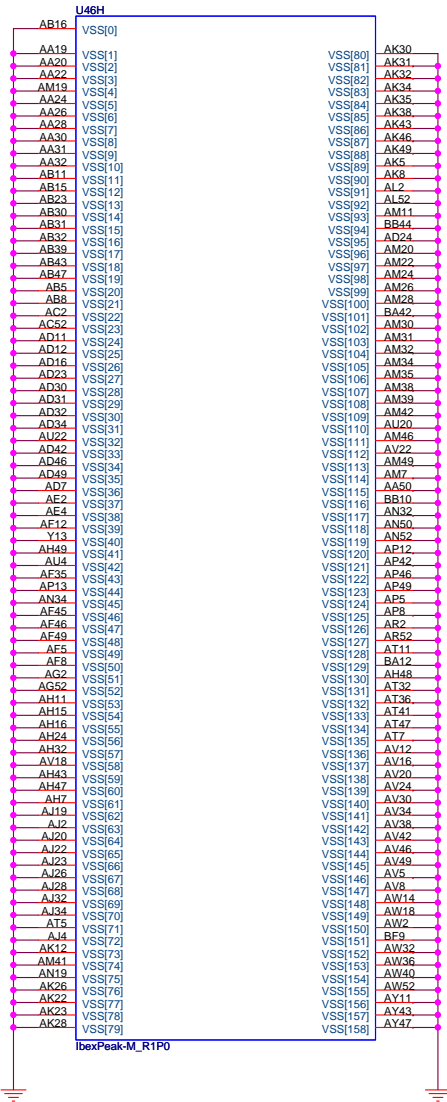
U46F



IBEX PEAK-M (POWER)



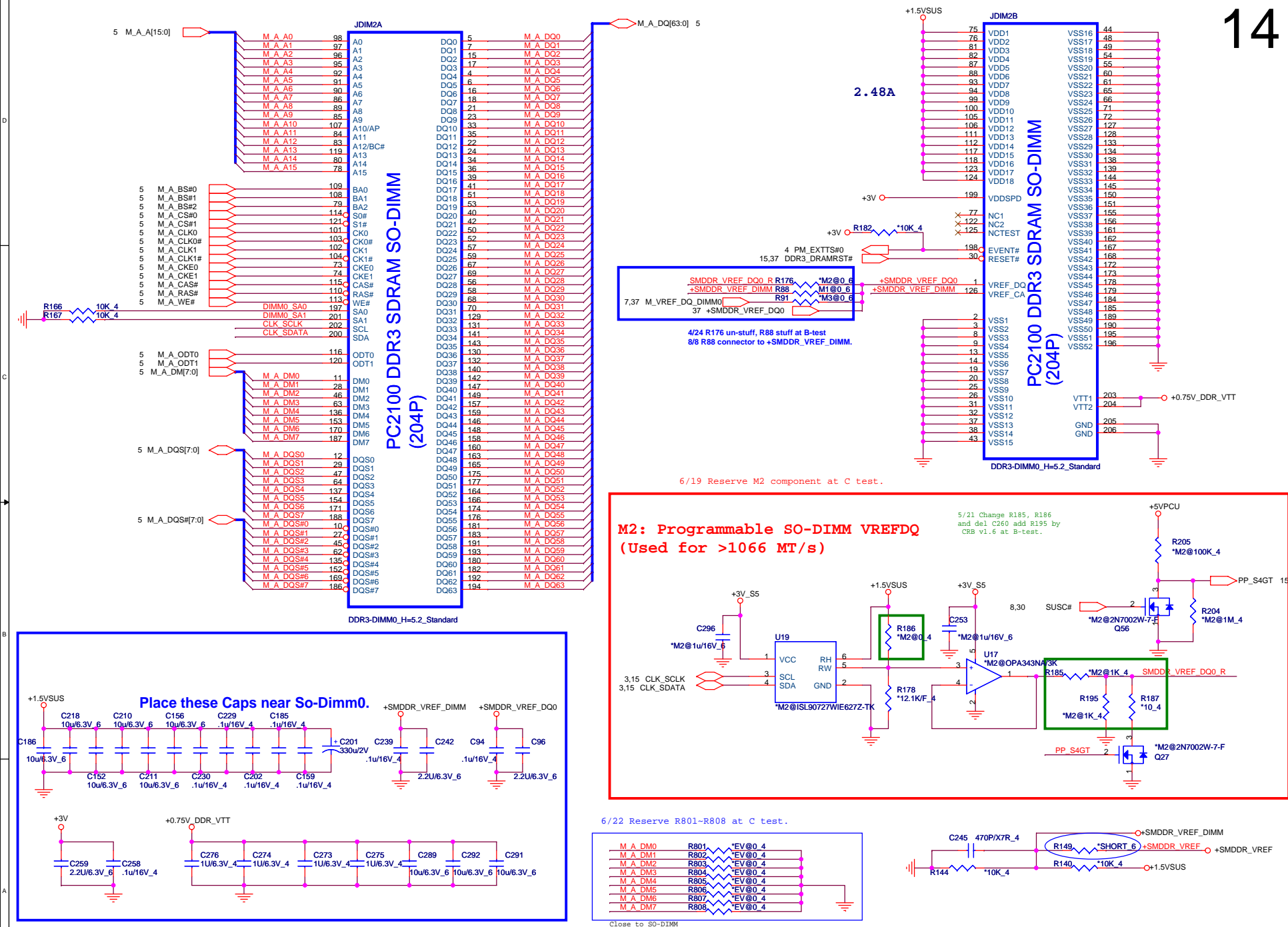
IBEX PEAK-M (GND)

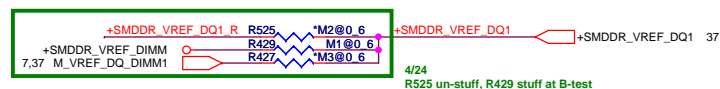
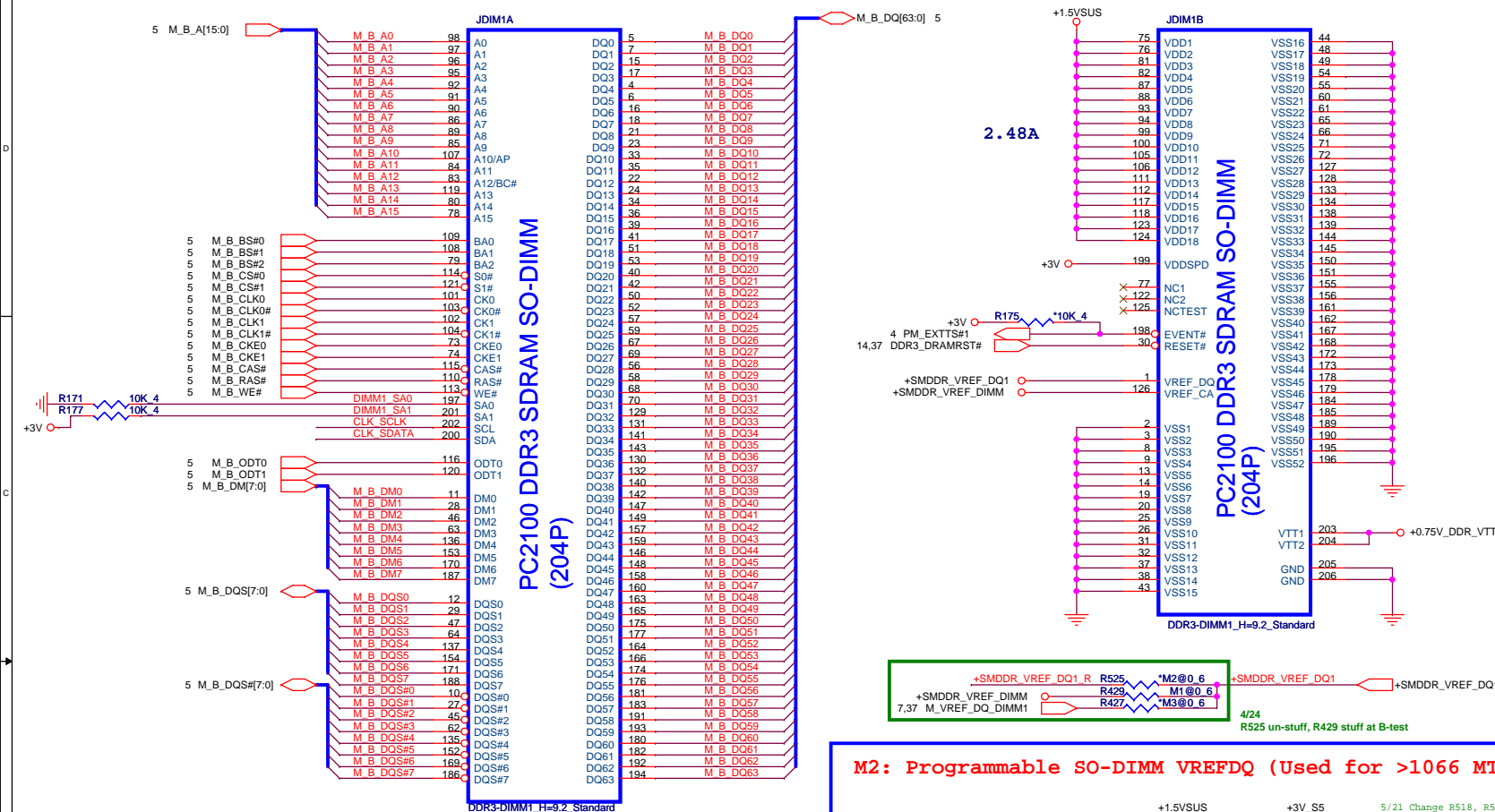


Quanta Computer Inc.

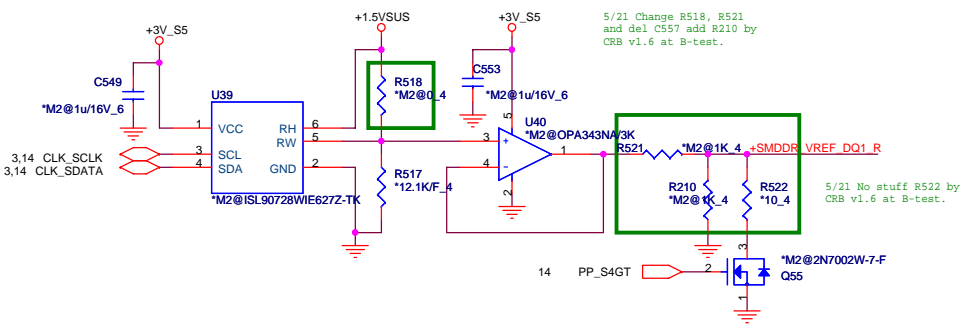
PROJECT : ZY9

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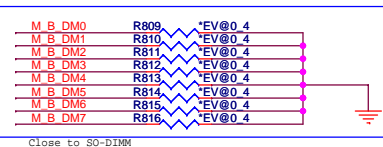


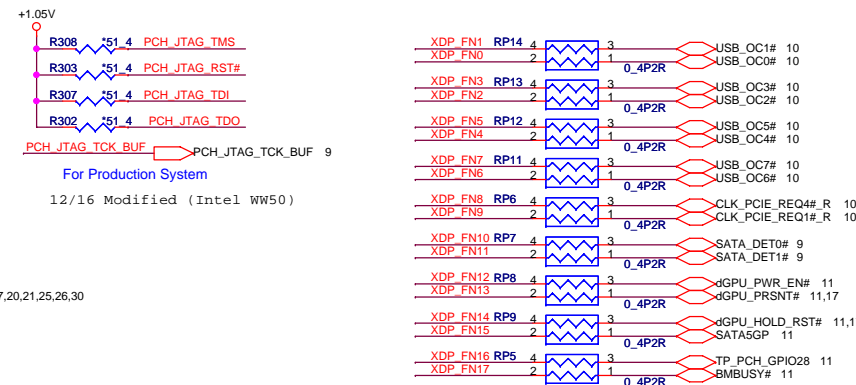
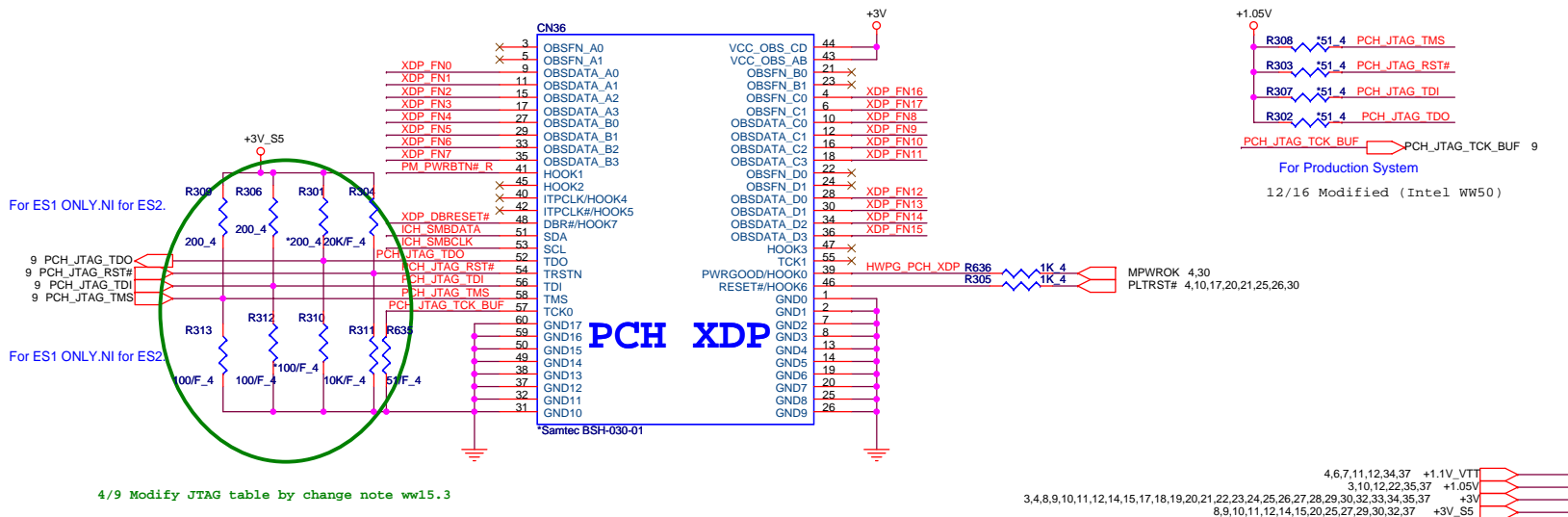
M2: Programmable SO-DIMM VREFDQ (Used for >1066 MT/s)



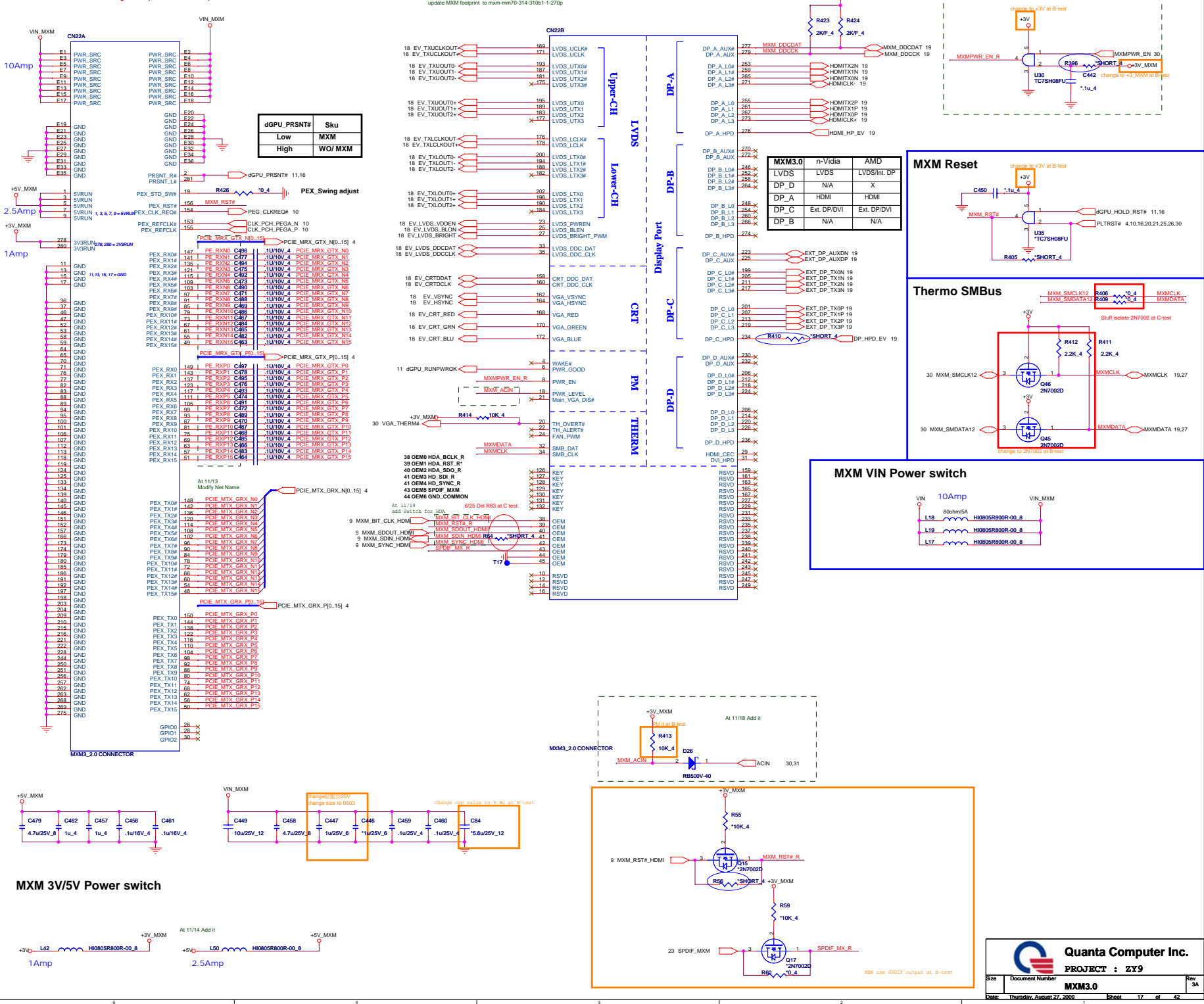
6/19 Reserve M2 component at C test.

6/22 Reserve R809-R816 at C test.





MXM Module 6/25 Change CN22 pin define and footprint at C test.



HDMI **TMDS (DC-coupled)**
DP (AC-coupled)

17 HDMICLK- **HDMICLK-** C77 1u_4 HDMI_CLK- **HDMI_CLK-**
17 HDMICLK+ **HDMICLK+** C90 1u_4 HDMI_CLK+ **HDMI_CLK+**

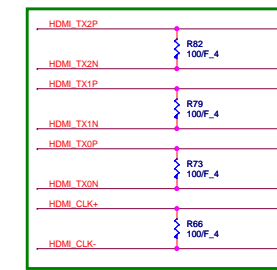
17 HDMITX0N **HDMITX0N** C83 1u_4 HDMI_TX0N **HDMI_TX0N**
17 HDMITX0P **HDMITX0P** C86 1u_4 HDMI_TX0P **HDMI_TX0P**

17 HDMITX1N **HDMITX1N** C87 1u_4 HDMI_TX1N **HDMI_TX1N**
17 HDMITX1P **HDMITX1P** C89 1u_4 HDMI_TX1P **HDMI_TX1P**

17 HDMITX2N **HDMITX2N** C90 1u_4 HDMI_TX2N **HDMI_TX2N**
17 HDMITX2P **HDMITX2P** C92 1u_4 HDMI_TX2P **HDMI_TX2P**

R86 499F_4 R83 499F_4 R81 499F_4 R78 499F_4 R76 499F_4 R69 499F_4 R67 499F_4 R65 499F_4

3V+ R92 100K_4 Q20 2N7002



The schematic shows two NPN transistors, Q47 and Q43, both labeled as 2N7002D. The base of Q47 is connected to a +3V supply through a resistor R415 (10K_4). The emitter of Q47 is grounded. The collector of Q47 is connected to the HDMI_HP_EV signal input. The base of Q43 is connected to a +3V supply through a resistor R404 (10K_4). The emitter of Q43 is grounded. The collector of Q43 is connected to the HDMI_HPD_INT# signal output. Both transistors are also connected to a common node labeled At 11/13, which is annotated with "Add HDMI hot plug to GPU". A charge source is indicated at the top right, connected to a node labeled At 11/18.

MXM DDCCK
MXM DDCDAT

R425 1.5K_4 *SHORT_4 EV_HDMICLK
R425 1.5K_4 *SHORT_4 EV_HDMIDAT

+5V
C455 22uF

U36
VCC GND
16 8
2 4
17 18
19 20
21 22
23 24
25 26
27 28
29 30

17 MXM DDCCK
18 MXM DDCDAT

17.27 MXMICLK
17.27 MXMDATA

6/30 Modify at C-test

9 dGPU_EDIDSEL#

S Yn
0 EV
1 IV

EV_HDMICLK
EV_HDMIDAT

2N7002D Q51
3 MB_HDMI_DDCCLK
4
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27
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29
30

+5V
D29 BAS316
R425 1.5K_4
+5V
D27 BAS316
R419 1.5K_4

NV suggestion near HDMI connector

HDMI_DDCCLK
HDMI_DDCDATA

L35 BLM18AG601SN1D_6
L34 BLM18AG601SN1D_6
C454 1uF
C452 1uF

2N7002D Q50
3 MB_HDMI_DDCDATA

Figure 10 shows the pin connections for the RCLink module. The connections are as follows:

- U8 (HDMI Connector):**
 - HDMI CLK+ to Pin 1
 - HDMI CLK- to Pin 2
 - HDMI DDDCLK to Pin 3
 - HDMI DDDATA to Pin 4
 - GND_3/8 to Pins 5, 6, 7, 8, 9, 10
- U10 (HDMI Connector):**
 - HDMI TX2P to Pin 1
 - HDMI TX2N to Pin 2
 - GND_3/8 to Pins 3, 4, 5, 6, 7, 8, 9, 10
- U9 (DVI Connector):**
 - HDMI TX0P to Pin 1
 - HDMI TX0N to Pin 2
 - GND_3/8 to Pins 3, 4, 5, 6, 7, 8, 9, 10

The RCLink module is connected to the RCLink module via the RCLink module.

[illegible]

DP Hot-PLUG to SB and GPU

The schematic diagram illustrates the DP Hot-PLUG circuit, which interfaces the DP_HPD_EV signal with the DP_AUXN and DP_AUXP signals. The circuit is powered by +3V_M00M and +3V.

DP_AUXN and DP_AUXP Paths:

- The **DP_AUXN** path uses MOSFETs Q38 and Q37 (2N7002D) and capacitors C439 and C441 (1uF) to interface with the **EXT_DP_AUXDN** signal.
- The **DP_AUXP** path uses MOSFETs Q39 and Q40 (2N7002D) and capacitors C439 and C441 (1uF) to interface with the **EXT_DP_AUXDP** signal.

DP_HPD Path:

- The **DP_HPD** path uses MOSFETs Q35 and Q36 (2N7002D) and a resistor R390 (10K_4) to interface with the **DP_HPD_EV** signal.

The circuit is powered by +3V_M00M and +3V. The DP_AUXN and DP_AUXP signals are connected to the DP_AUXN and DP_AUXP pins of the DP connector. The DP_HPD signal is connected to the DP_HPD pin of the DP connector.

DP1

U5

1	2	3	4
1	2	3	4
10	9	7	6

EXT DP TX2
EXT DP TX2
EXT DP TX3
EXT DP TX3

RClamp0524P

DP2

U6

1	2	3	4
1	2	3	4
10	9	7	6

EXT DP TX0
EXT DP TX0
EXT DP TX1
EXT DP TX1

RClamp0524P

U4

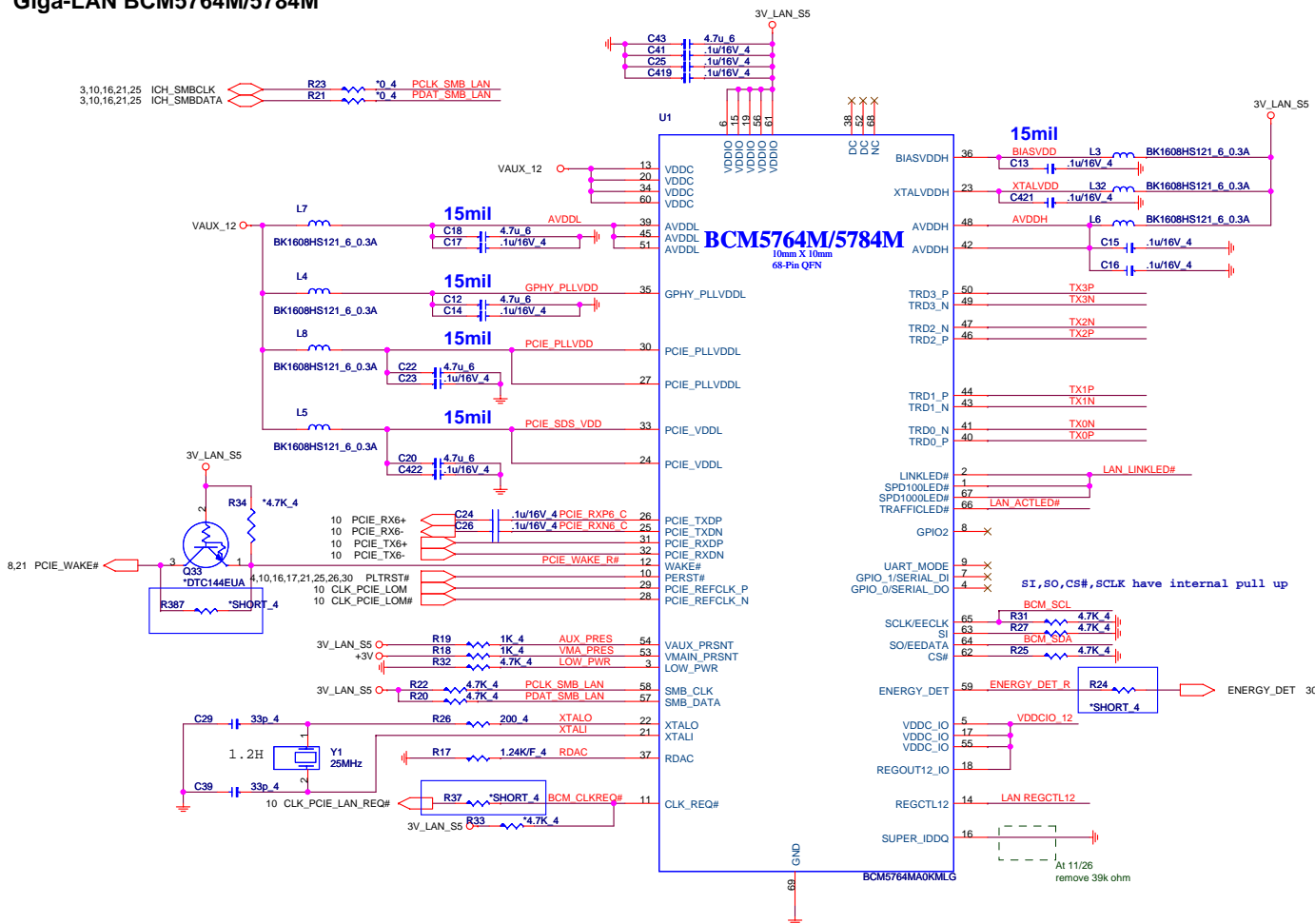
1	2	3	4
1	2	3	4
10	9	7	6

DP AUXP
DP AUXN
DP CAD
DP HPD

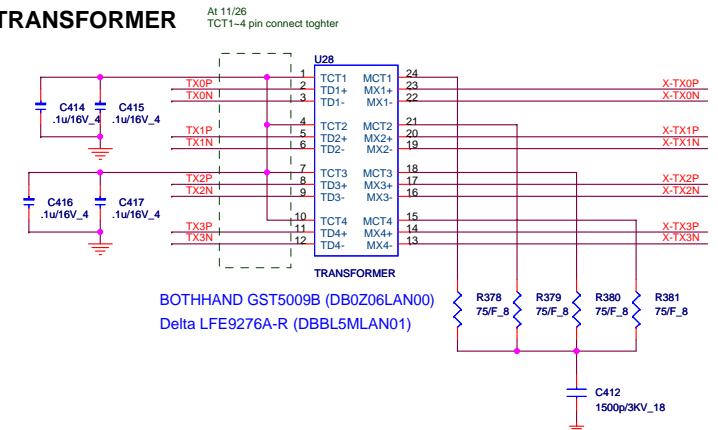
RClamp0524P

DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDs signal (DC couple)

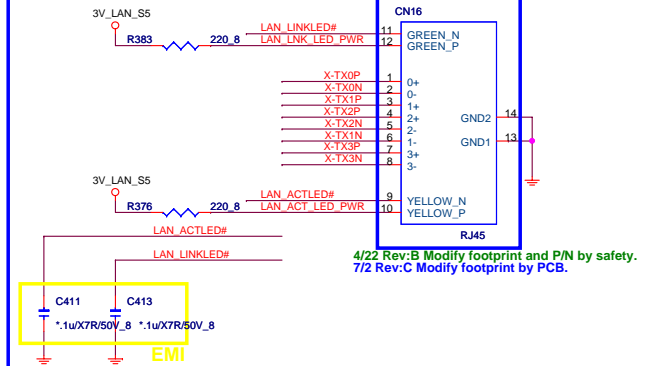
Giga-LAN BCM5764M/5784M



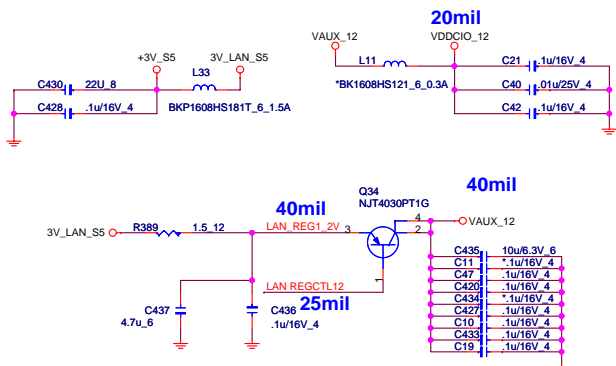
TRANSFORMER



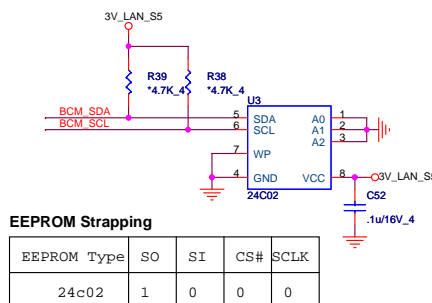
RJ45



LAN POWER

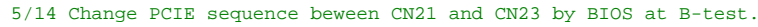


EEPROM

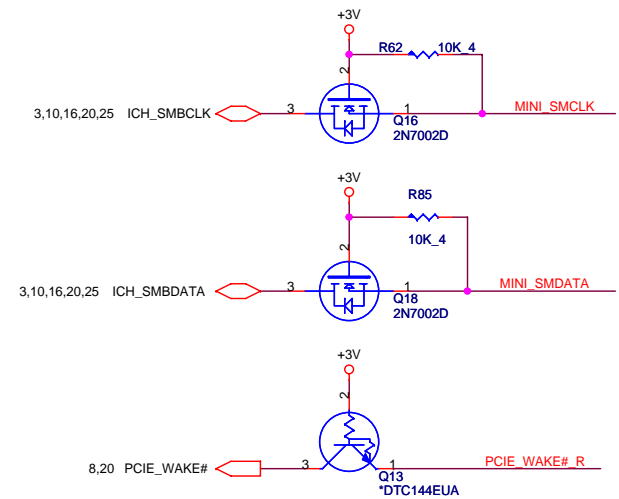



Modify to 2Conn. at B-test

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

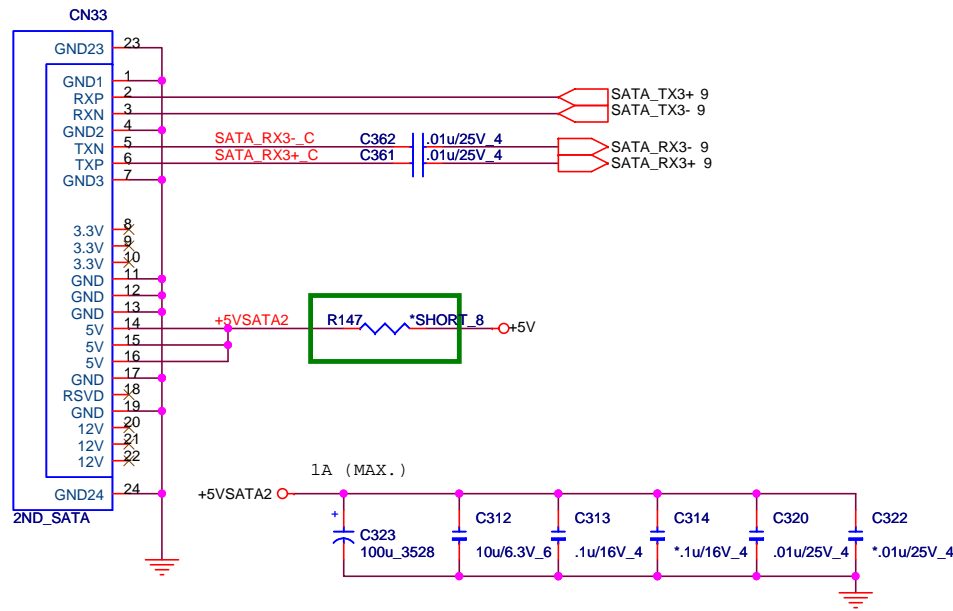


350mA, 20mil

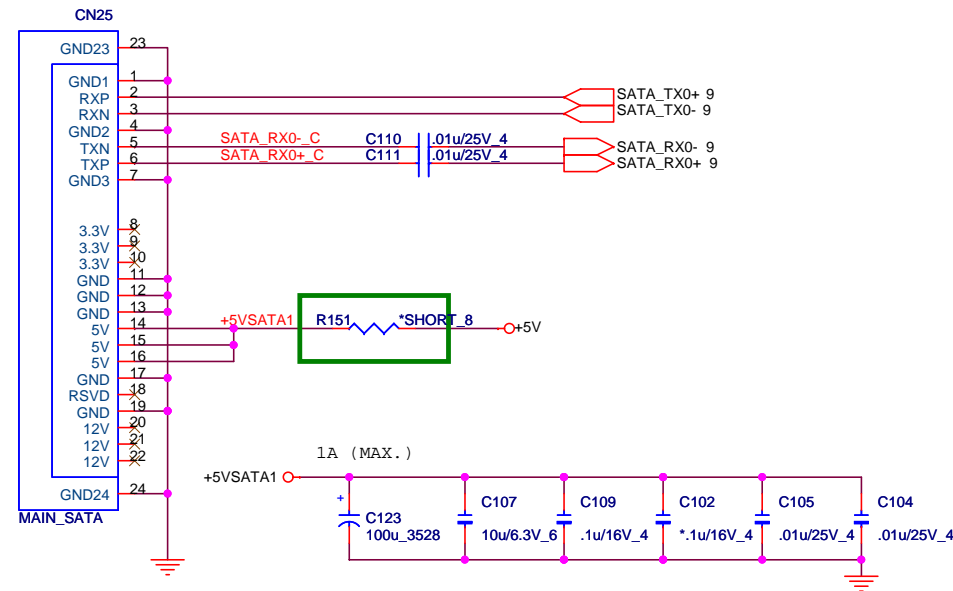


 Quanta Computer Inc. PROJECT : ZY9		Rev 3A
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MINI PCI-E card/TV		
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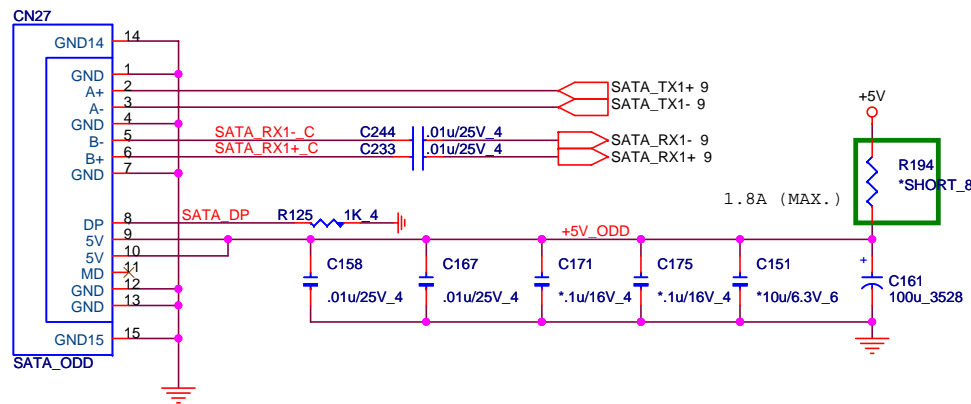
2nd SATA HDD (edge of board)



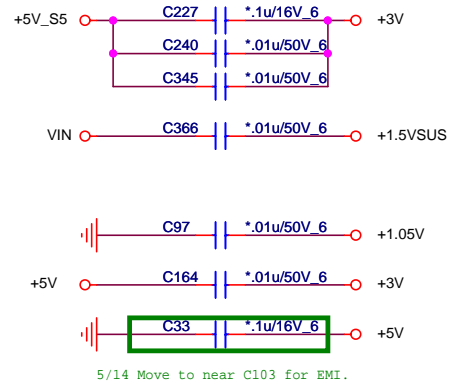
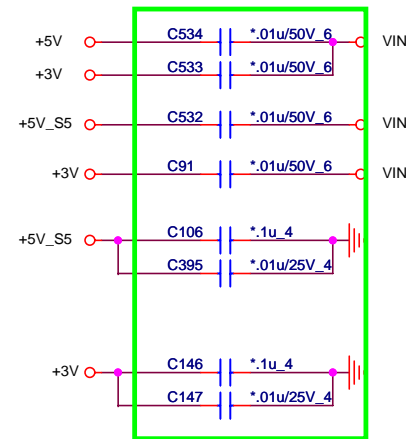
MAIN SATA HDD



ODD (SATA)



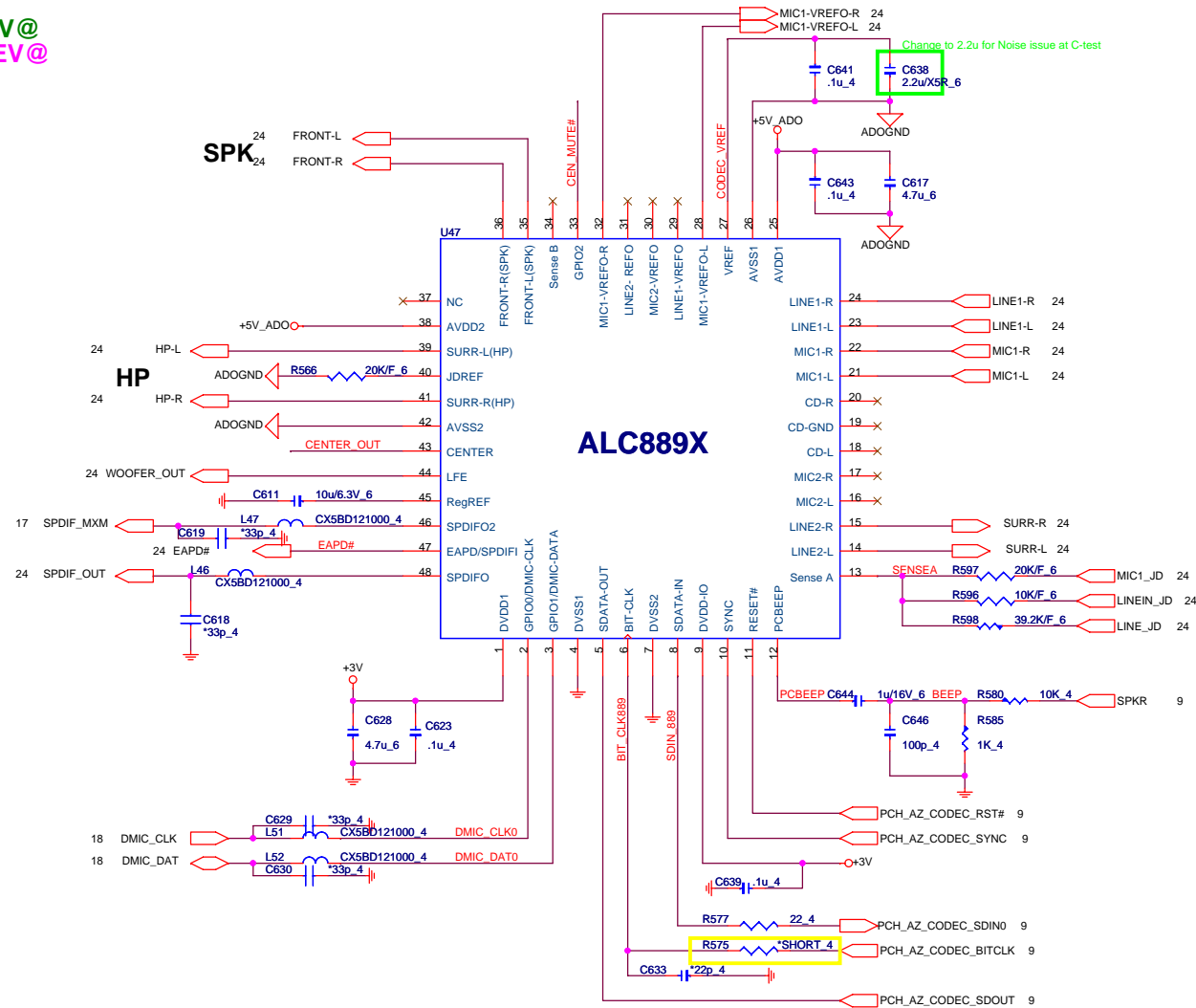
EE RETURN-PATH CAPACITORS



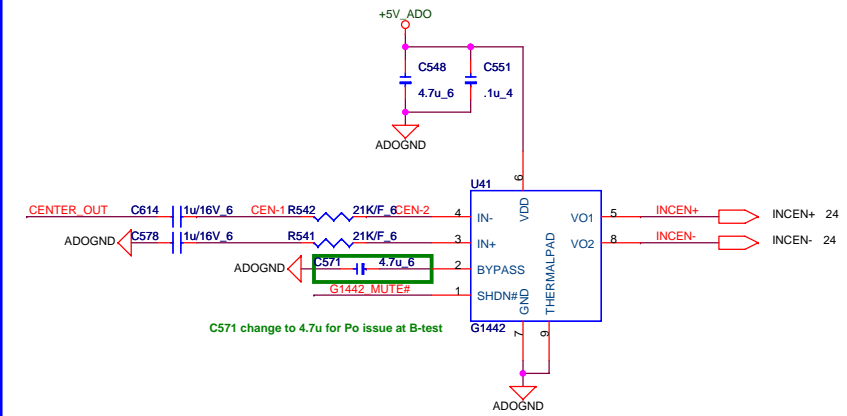
Quanta Computer Inc.
PROJECT : ZY9
SATA-HDD/ODD

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CODEC(ALC889X)

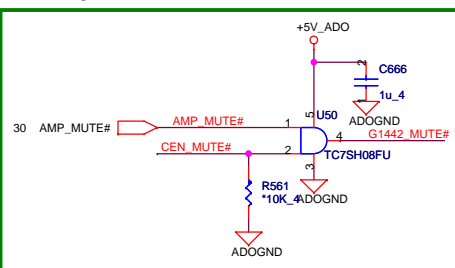
IV@
EV@

CENTER MONO

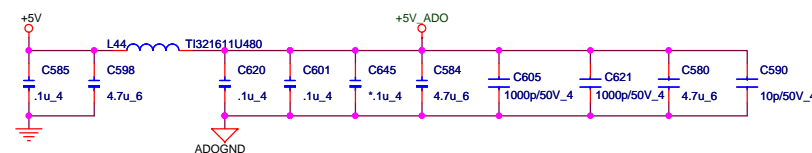


EAPD pin

5/11: Add U50, C666 and R561 for Po issue at B-test



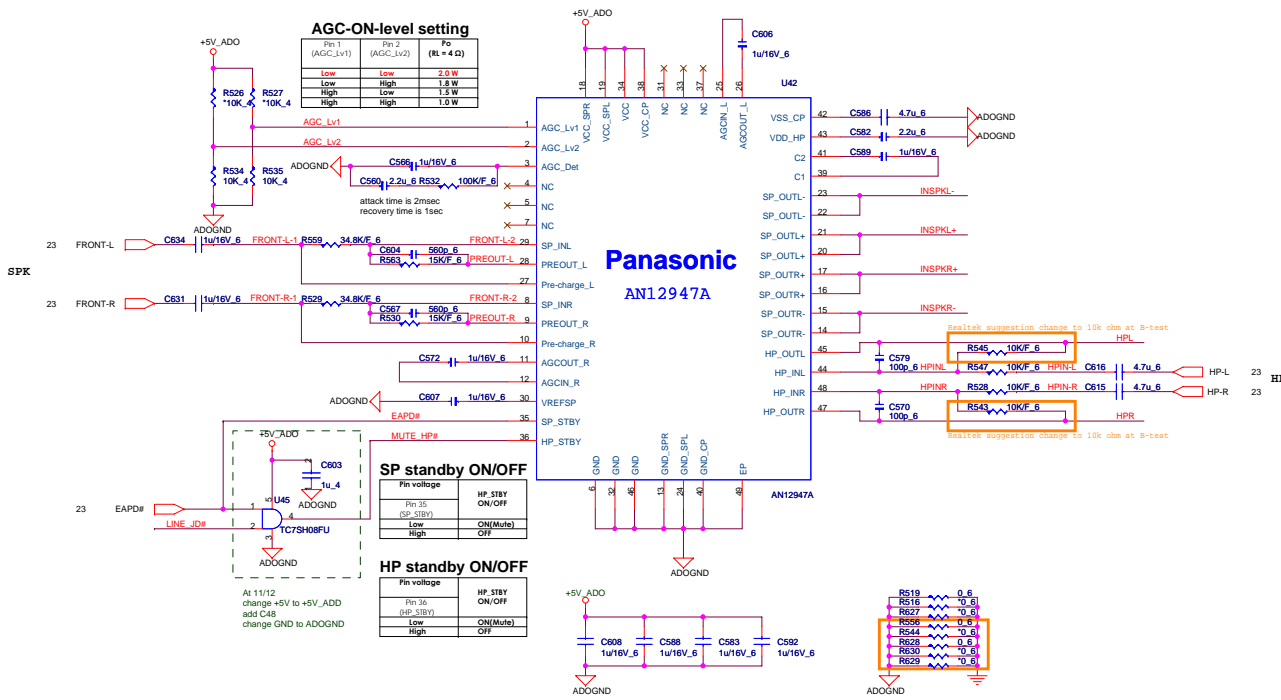
CODEC/AMP Power



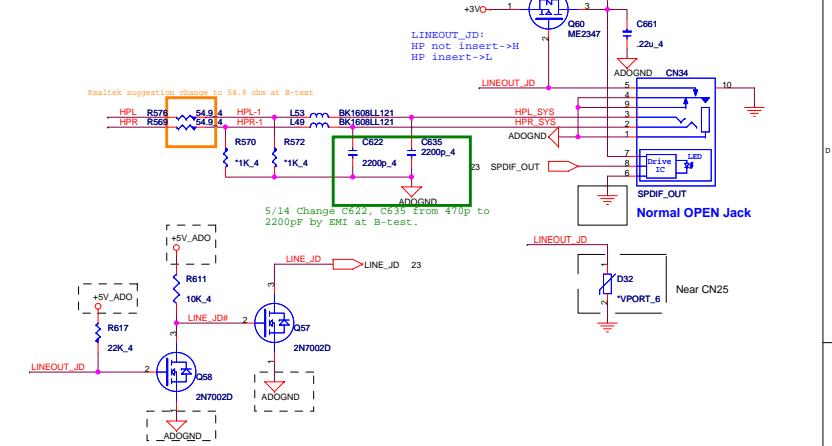
Quanta Computer Inc.
PROJECT : ZY9

Size Document Number
REALTEK ALC889X/MONO-AMP
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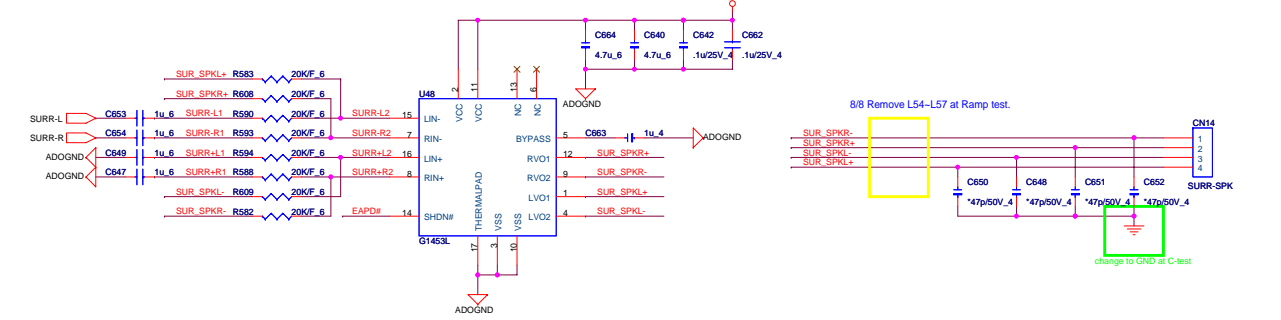
SPEAKER/HP AMP.



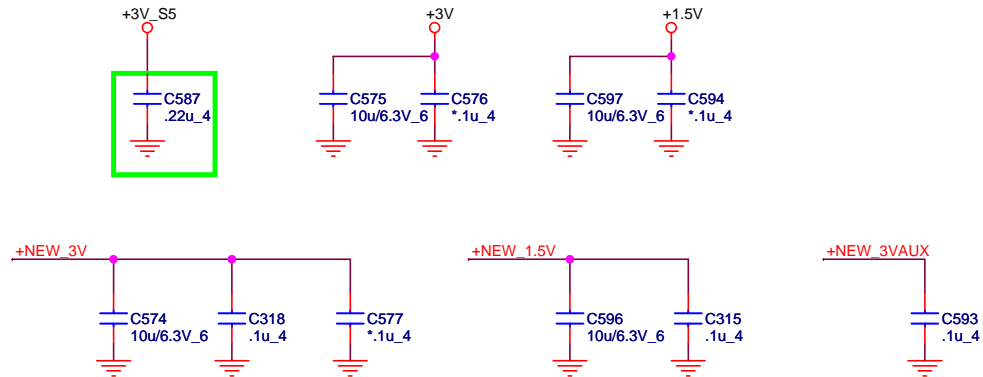
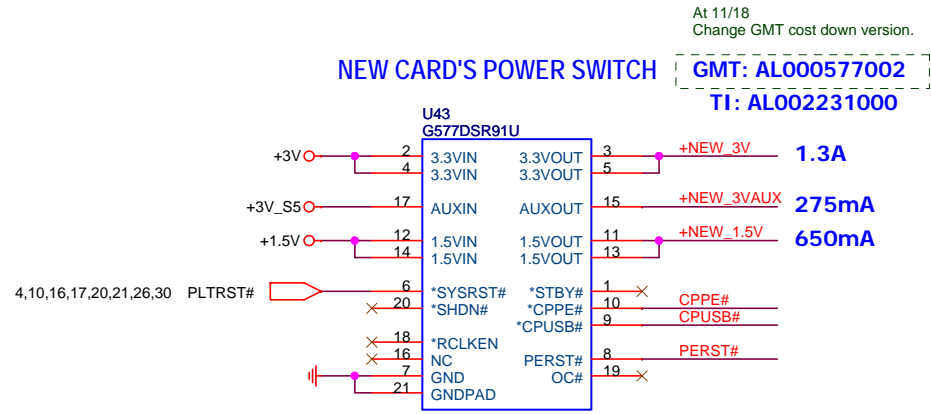
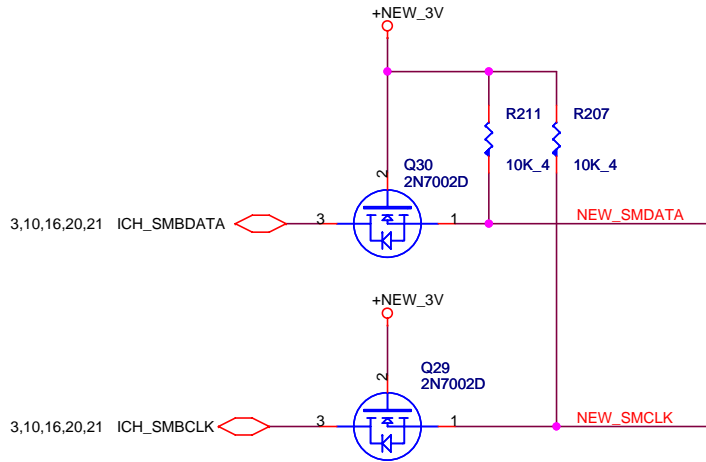
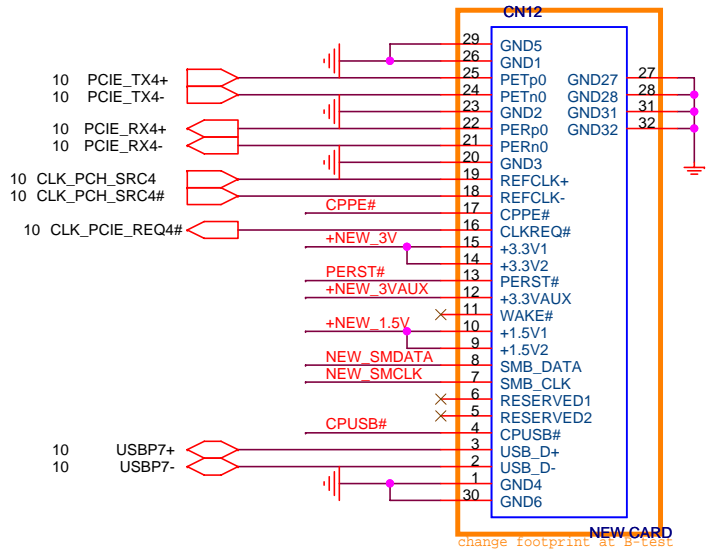
LINE-OUT/SPDIFO



SURR-SPK

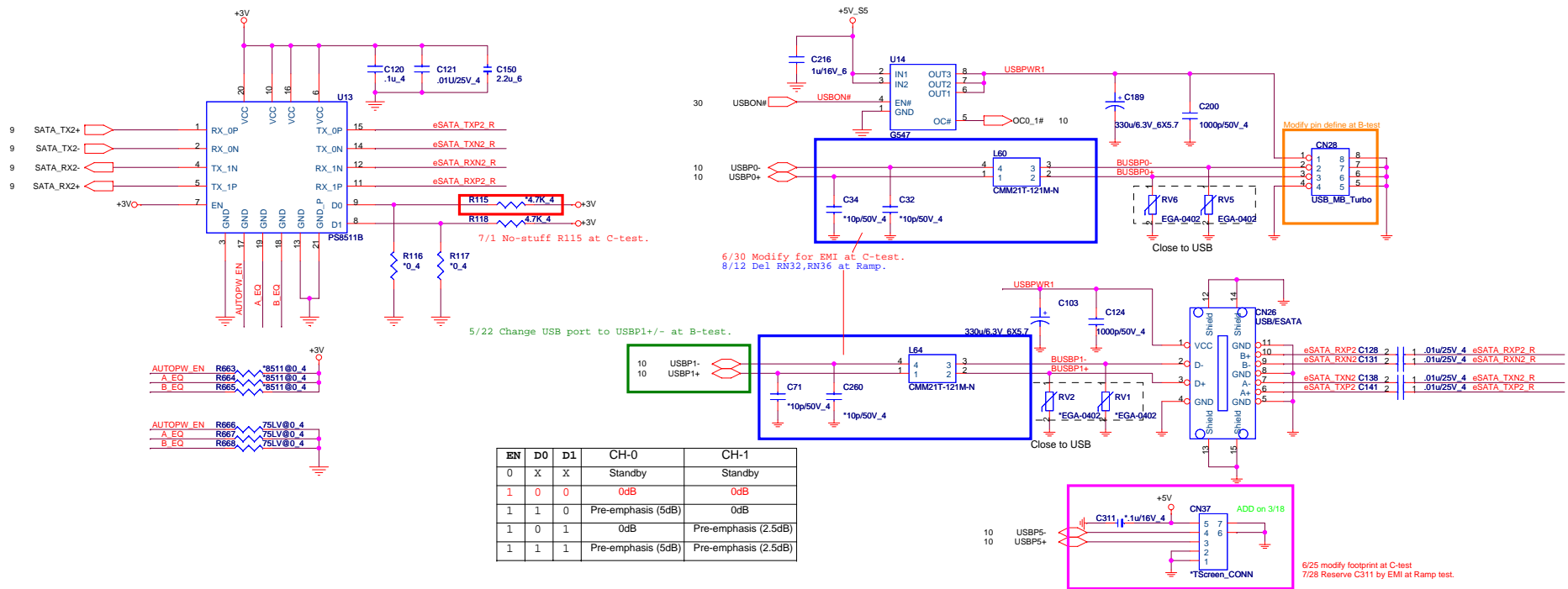


NEW CARD

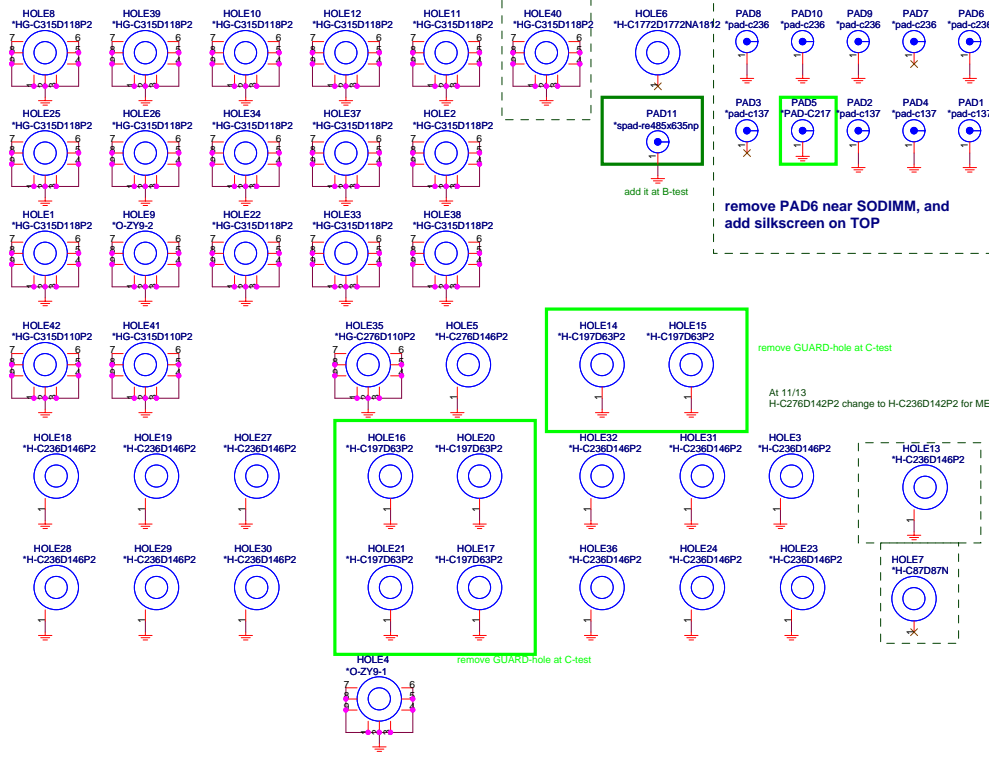




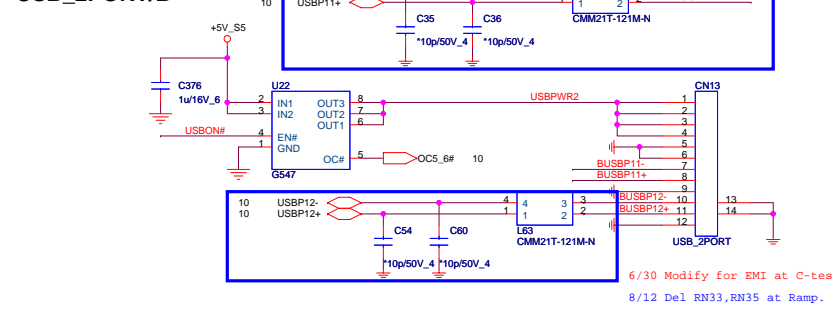
USB & ESATA



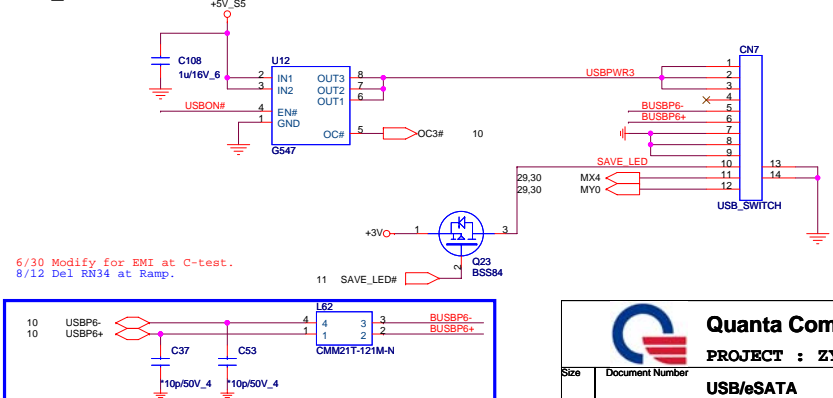
HOLES



USB_2PORT/B

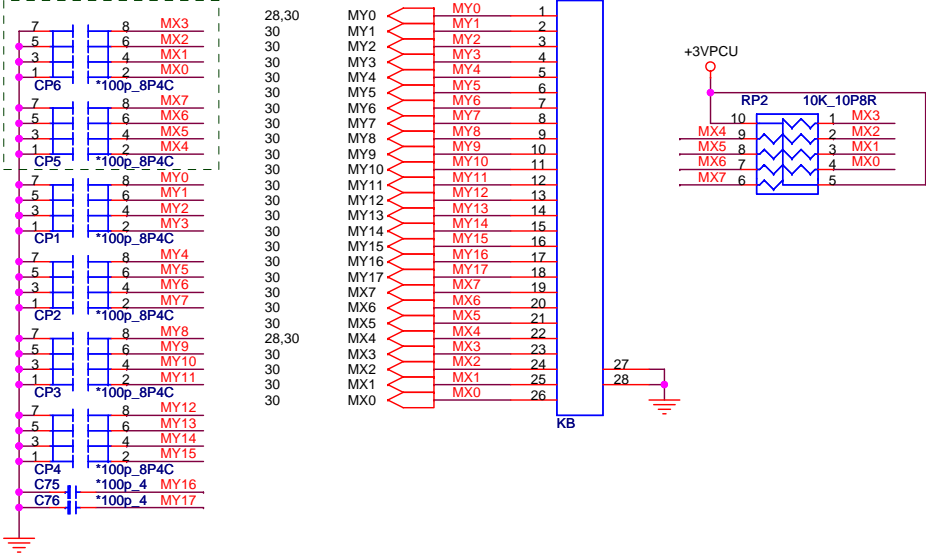


USB_SWITCH/B

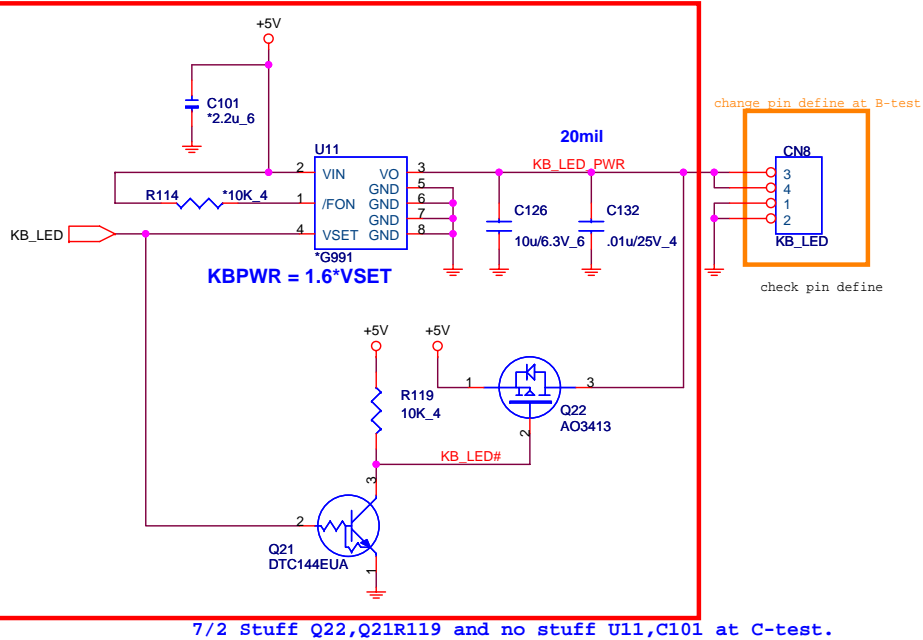


INT K/B

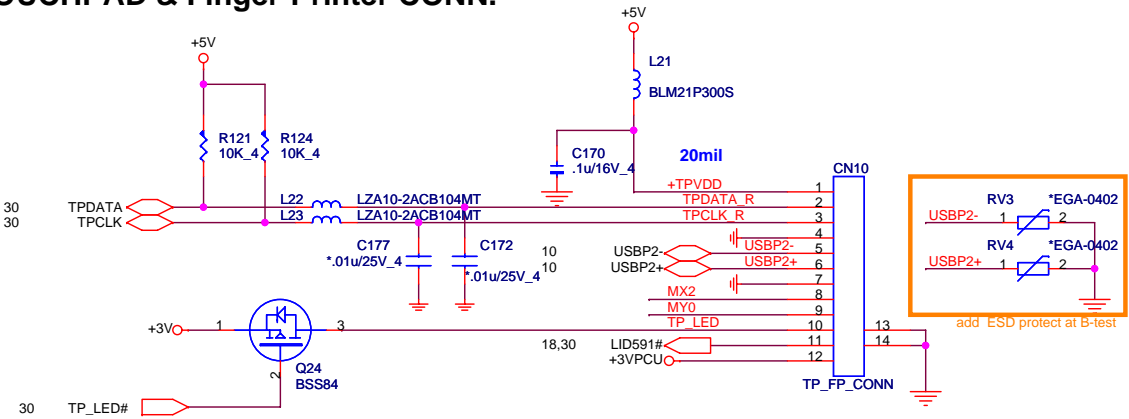
At 11/18
SWAP



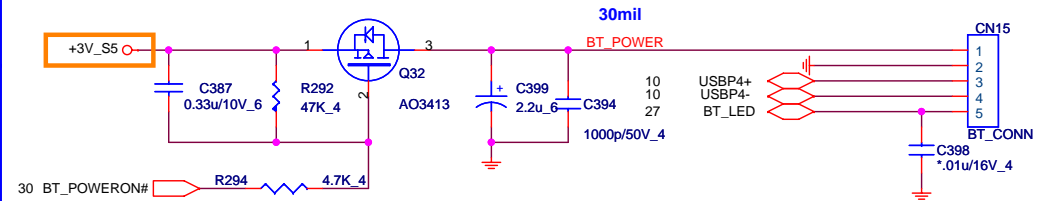
Keyboard LED control



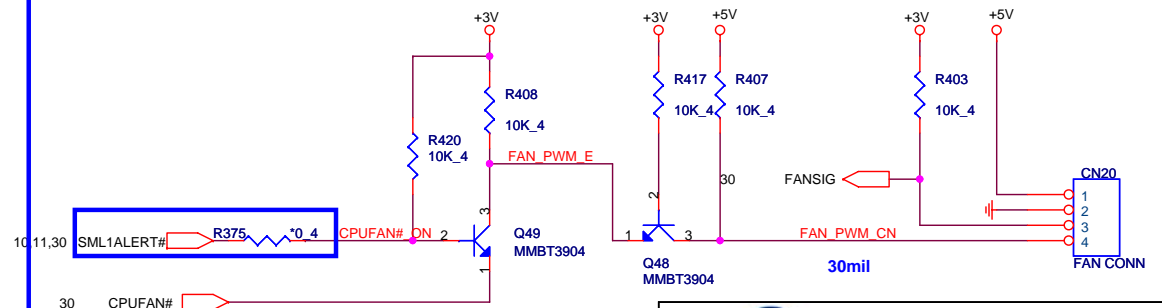
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



CPU FAN



5/13 Reserve R375 by EC at B-test.

6/25 Stuff R375 by EC at C-test.

7/22 Un-stuff R375 by EC at Ramp.



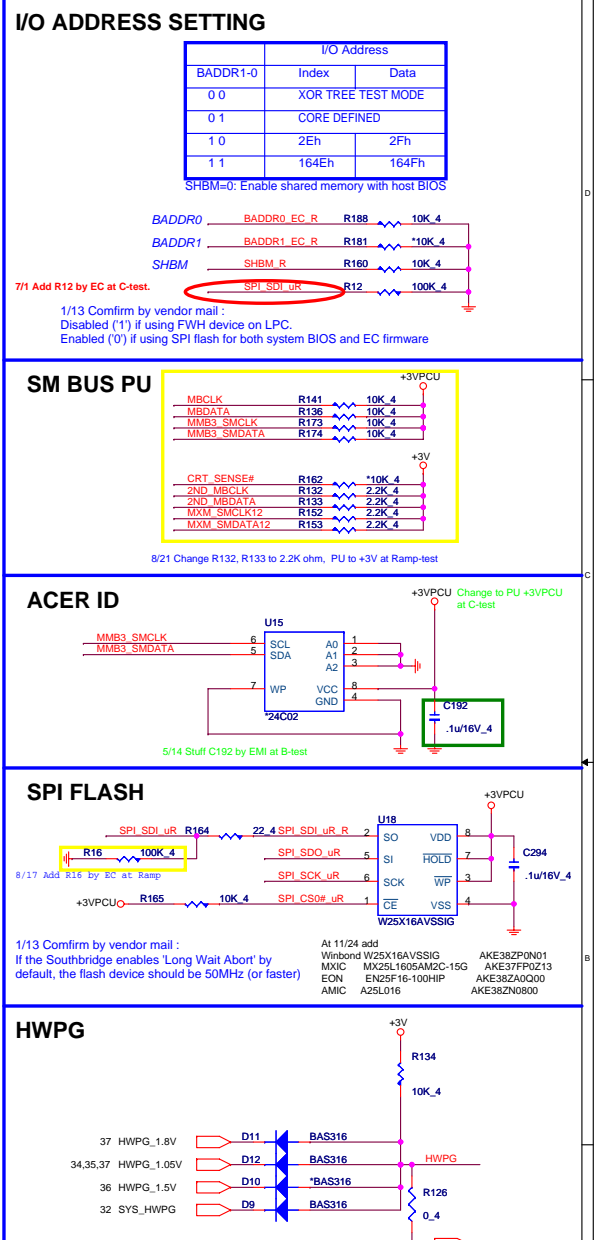
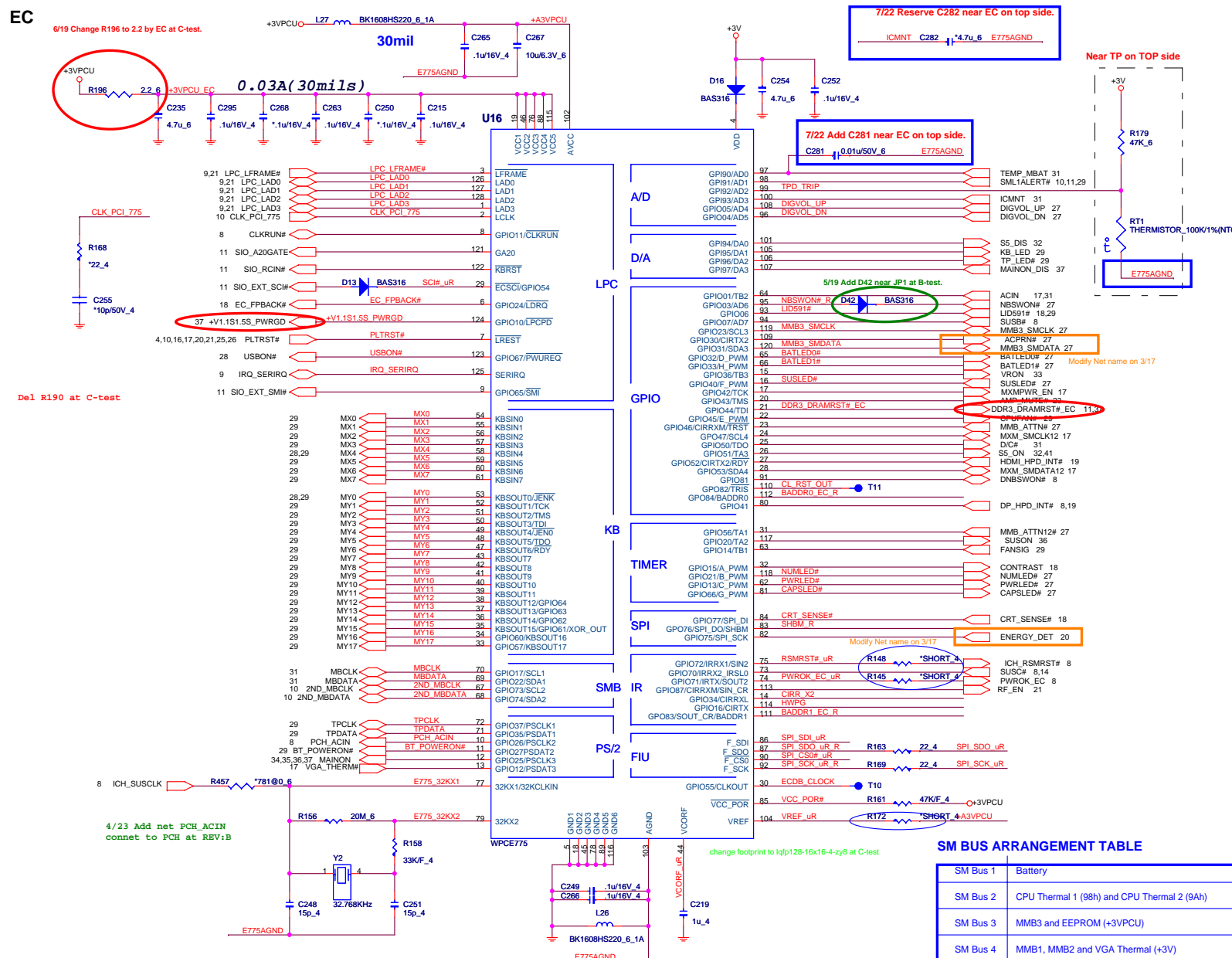
Quanta Computer Inc.

PROJECT : ZY9

KB/FAN/TP+FP/BT

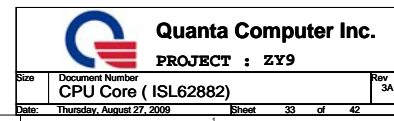
Size	Document Number	Rev
	KB/FAN/TP+FP/BT	3A
Date:	Thursday, August 27, 2009	Sheet 29 of 42

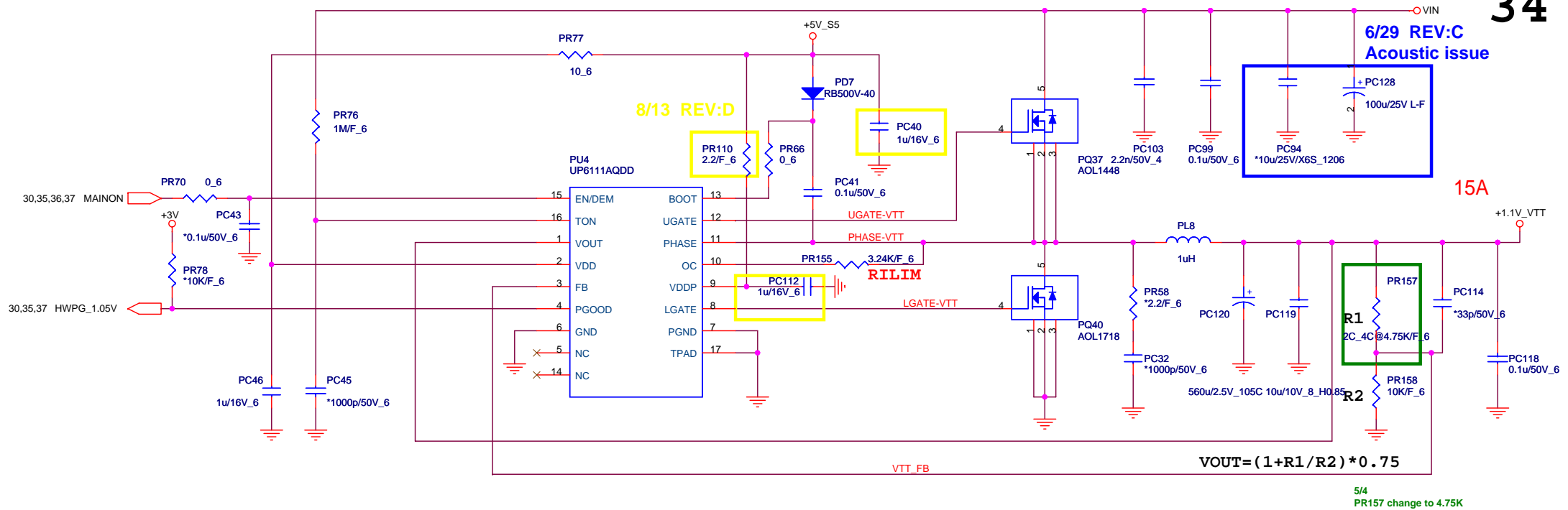
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AO1718 Rdson=3~4.3mOhm

Aurbundale (1.05V) R1 = 4.02K (CS24023F928)

Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

L(ripple current)
= (19 - 1.05) * 1.05 / (1u * 272k * 19)
~ 3.64A

4.3m * 15 = RILIM * 20uA
RILIM = 3.24K (3.22K)

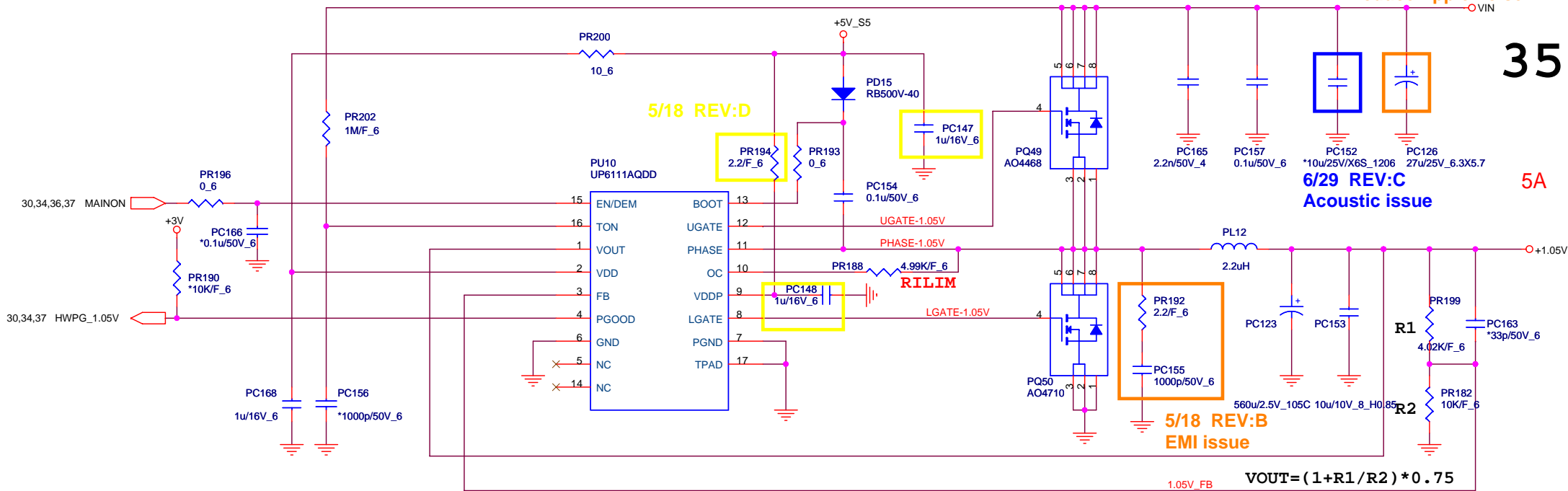


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PROJECT : ZY9

Size	Document Number	Rev
	+VTT (UP6111A)	3A
Date:	Thursday, August 27, 2009	Sheet 34 of 42

[PWM]

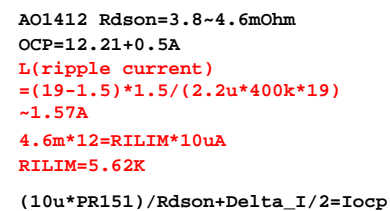


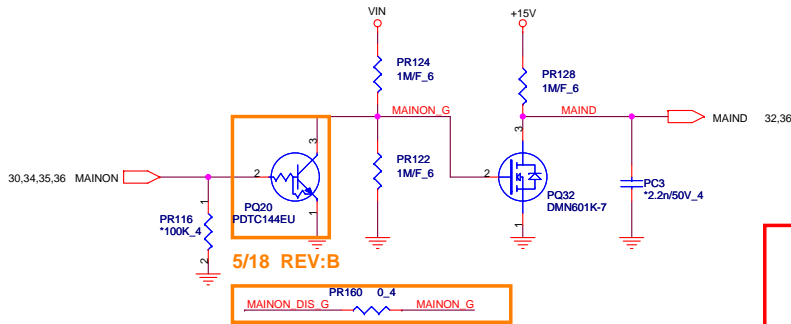
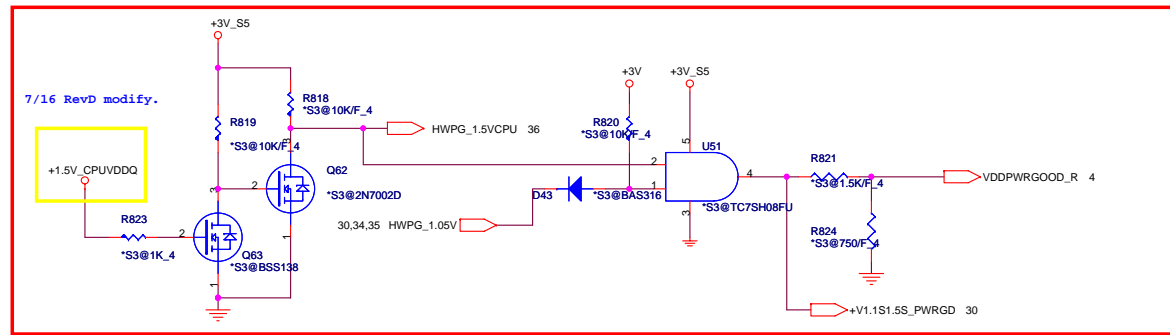
AO4710 $R_{dson}=11.8\sim14.2m\Omega$
 OCP=7.2-0.8A
 $L(\text{ripple current})$
 $= (19-1.05) \times 1.05 / (2.2u \times 272k \times 19)$
 $\sim 1.6577A$
 $14.2m \times 7 = RILIM \times 20uA$
 $RILIM = 4.99K (4.97K)$

Quanta Computer Inc.

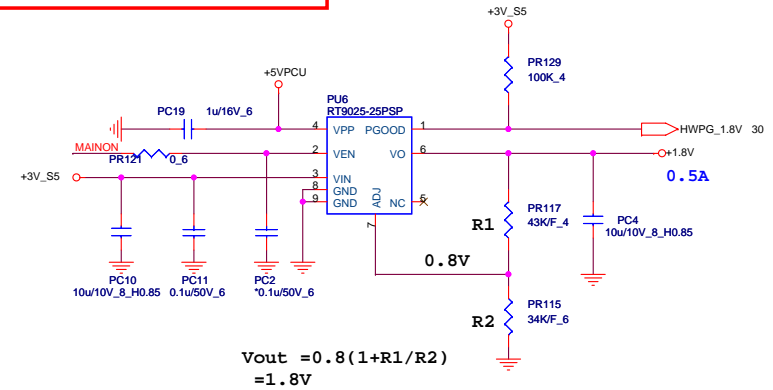
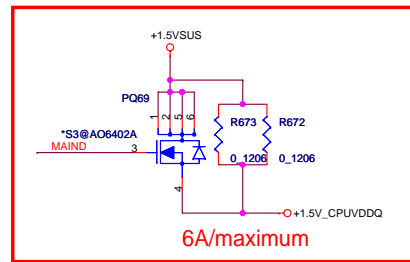
PROJECT : ZY9

Size	Document Number +1.05V(UP6111AQDD)	Rev 3A
Date:	Thursday, August 27, 2009	Sheet 35 of 42

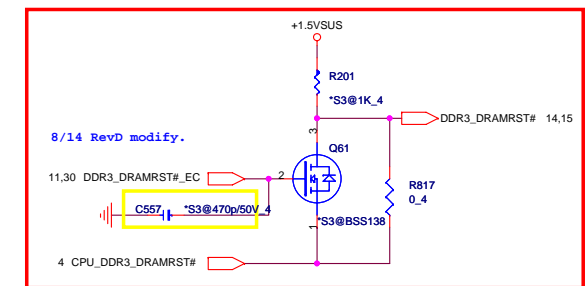
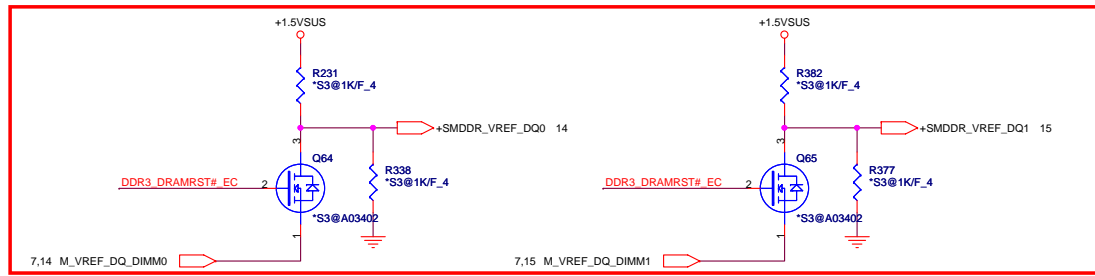
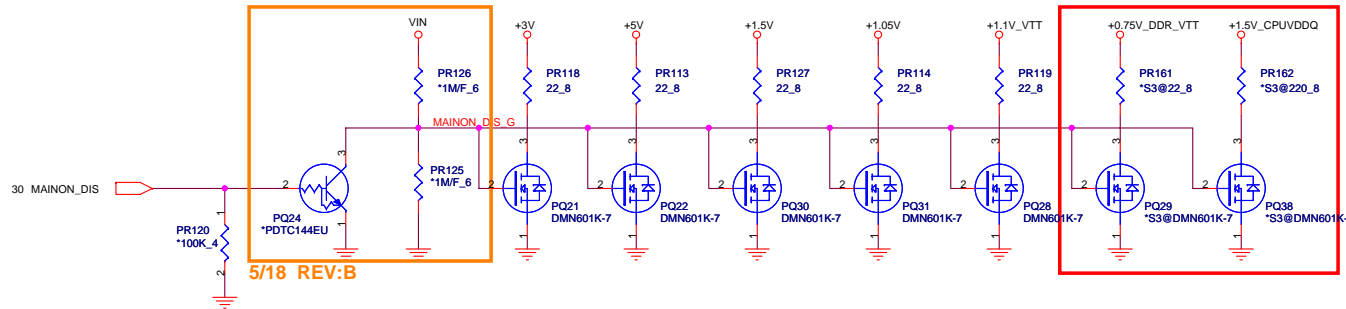
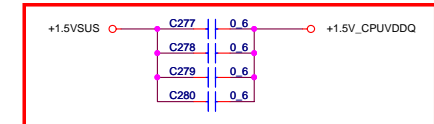




5/25 stuff PR160, no stuff PQ24, PR126, PR125 at B test.



S3 power solution: C277~C280 stuff 0.1uF cap;
Normal : Stuff 0ohm to short.



12,21,25,36 +1.5V
6 +1.5V_CPUVDDQ

